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Adynamic Imbalanced Load Modulation Approach To Design And Implement An Energyefficient RF Power Amplifier

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---ABSTRACT---

In this paper, a dynamic load modulation approach using an attenuator has been presented to design a concept of energy efficient class-AB RF power amplifier for modern wireless communication systems. The output power back off technique is to amplify the signal at the linear region to keep away from unwanted spurious. However, the use of dynamic load modulation approach causes excessive increase in PAE, drain efficiency and P_{out}.To improve the efficiency at wide range of output power and possess similar margin for signal with high crest factor, the dynamic load modulation technique with an offset line are introduced to operate over power amplifier load modulation technique. The dynamic load modulation technique is compared with balanced power amplifier technique to find a best candidate. A simulation results achieved from the dynamic load modulation power amplifier with 79% power added efficiency at 35dBm output power. The result has shown reasonable improve from dynamic load modulation over the balance power amplifier design.

KEYWORDS: *Power Amplifiers, Class-AB, Class-C, Efficiency, Linearity.*

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I. INTRODUCTION

Wireless communication systems are becoming more prevalent over the years. These systems continue to accelerate growth in providing diverse multimedia services for more wireless service users. The exponential growth of service users, make the system become more complex and however induce inefficient usage of limited available RF spectrum resource. New generation wireless communication systems are complex modulation based and require high speed data rate to support the demand for multimedia services. Modern wireless communications systems such as Long Term Evolution (LTE), Wireless local Area Network (WLAN) and Worldwide Interoperability for Microwave Access (WiMAX) support adaptation of energy efficient transmitter, targeted for high capacity and high transmission speed. The high transmission data rate, of course, anticipates the use of bandwidth efficient modulation techniques such as Orthogonal Frequency Division Multiplex (OFDM) and Quadrature Phase Shift Keying (QPSK). However, these spectral efficient modulation schemes require high power efficiency with maximum linearity from power amplifier device itself[1].

Modulation schemes such as OFDM and WCDMA acquire intense constellation diagrams using multiple access technique. These are exposed to nonlinear distortion due to high peak to average power ratio (PAPR). PAPR is caused due to the envelop fluctuation of the modulation time-domain signals. The QPSK is also a bandwidth efficient modulation scheme, which requires amplifier linearity for spectral efficiency. Linear amplifier is traditionally a poor efficient device, having high cost of operation and requires heat sick due to excessive heat dissipation. Signals with high PAPR are drive in low efficiency. Nonlinear amplifier on the other hand distorts the constellation diagram of high PAPR signal, which led to increase in Adjacent Channel Power Ratio[2]. The ACPR is however measured based on the gravity of PAPR exhibited and typically by which application. For instance, Wideband CDMA and CDMA2000 exhibit up to 10dB PAPR, while OFDM will have a PAPR of around 17dB for WLAN IEEE 801.11a using a bandwidth of more than 20MHz[1, 2].

Power amplifiers are fundamental components in communication system transmitters. Due to nonlinearities, they generate nonlinear crosstalk which offset transmission process, and generate spectral re-growth.This behavior leads to interference and in-band distortion.The in-band distortion can affect the bit error ratio (BER) performance and produce out-of-band emission (CO2 emission). Power amplifier nonlinear distortion according to [3], can effectively be reduced by Power back-off and PAPR reduction techniques, but at the same time result in low power efficiency. Thus, a linear amplification is essential and can be obtained using linear amplifier or using nonlinear amplifier with the aid of linearization technique. Furthermore, power amplifier efficiency can effectively increase[4].

To achieve efficiency, linearity and high data rate for a modern energy efficient wireless communication transmitter, a linearization scheme and a trade-off between linearity and efficiency power amplifier need to be considered in this research. A class-AB amplifier can provide linearity and high efficiency. Another choice is a nonlinear class-F power amplifier which can however provides up to 80% power added efficiency. To linearize the class-F power amplifier, a pre-distortion system is required, while linearity and efficiency can be achieved. Consequently, there are futuristic energy efficient amplifier design techniques such as Balance Configuration[5], Doherty Configuration, Chireix out-phase, ET and Kahn EER. The most common and useful compensation techniques are feedback, feedforward, linear amplification with nonlinear components (LINC), envelope elimination and restoration technique (EERT) and different types of pre-distortion techniques. The state-of-the-art among all linearization techniques appears to be digital pre-distortion which can be cascaded at the baseband of the transmitter to linearize the output signal of a power amplifier. Similarly, a power amplifier can reach it saturation stage, maintaining an excellent linearity to increase efficiency when digital pre-distortion system is employed. But, this process, at time goes on will change the characteristics of the components and increase transistor thermal runaway, resulting to temperature drifting. Therefore, digital pre-distorter will take account of the changes and adapt[6].

The new method is demonstrated with a simulations operating at f_c = 3.50GHz with a 35dBm output power and 79% power added efficiency. These explained configuration of the circuit, characteristics of operation, linearity operating condition and optimal efficiency of the proposed method, which is presented in Section II. Design, simulation and results are described in III.

II. THE DYNAMIC LOADING DESIGN CONIDERATION

This paper considered a dynamic load modulation approach to improve the drain efficiency of a two transistors power amplifier. The dynamic load modulation approach is used in changing the load line matching at the output network of the power amplifier.The effect of this approach on the drain current and voltage can improve the performance of the power amplifier. By changing the load impedance at the output of a transistor increase the drain efficiency.Raab [7]clearly defined that dynamic load modulation is an approach that can be used to dynamically differentiate the load impedance of a power amplifier to produce amplitude modulation with high drain efficiency.

The dynamic load modulation can be applied on cascaded power amplifiers, i.e., a Doherty, balanced power amplifier, etc.The power amplifier consists of two transistors working harmonically as carrier class-AB power amplifier and peaking class-C power amplifier. A 90 degrees phase shift divider was employed to split the signal into two equal magnitudes[5, 8]. The combiner at the output of the two transistors, with a quarter wave impedance inverter, combines the output signal. The concept of dynamic load modulations allows the class-C transistor to pull the load presented to the class-AB transistor for high efficiency and output power.However, by providing the divider, the transistor of the peaking class-C will have more input signal passing through than the carrier class-AB. More input signal passing through the peaking transistor, turn on the class-C amplifier, while class-AB amplifier reaches the saturation region. Thisprocess of amplification protects the amplifier from power leakages between the peaking class-C and output load impedance transformer [8].

The imbalanced load modulation power amplifier operations depend on controlling the harmonics of the bias voltage and current to perform effectively. The diagram presented in figure 1 has been proposed for cascaded class-AB and class-C power amplifier. The theory of class-AB and class-C power amplifiers has been presented in [2]. The class-AB amplifier DC quiescent current is within the pinch off region, while class-C amplifier DC quiescent current iswithin the lower level of the threshold. Meaning that, the input signal at the peaking amplifier is at the low level and too insignificant to turn on the transistor which causes the peaking class-C amplifier to behave as an open circuit at the output. A quarter wave transmission lines at the carrier class-AB amplifier was employed to provide high impedance, as a result of the small signal, the amplifier run into saturation at maximum voltage condition.

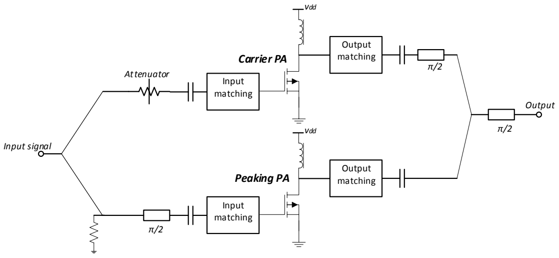

Figure 2: Dynamic imbalance load modulation power amplifier configuration.

The characteristic impedance of a quarter wave transmission line can be derived as:

$$Z_{in}=\frac{Z_0^{\ 2}}{Z_{out}} \qquad (1)$$

where z_{in} and z_{out} are the respective input and output impedances, while z_o is characteristic impedance of the transmission line. From the equation, carrier class-AB amplifier saturation level increases when input signal increases. The peaking class-C amplifier bias network will be at active stage and the bias current will flow to the transistor output, while increasing the characteristic impedance, z_o. Impedance of the input signal reduces due increase in characteristic impedance. Furthermore, as a result of decrease in z_{in}, the carrier class-AB amplifier becomes disabled and will not perform. At the same time, the peaking class-C amplifier will be on, until reach a saturation point. Both carrier and peaking amplifiers will be at the terminating load impedance, $2R_L$. This has been illustrated from the figure that the amount of power passing through class-AB to the load is the same equal amount of power passing through the peaking amplifier to the same load impedance as illustrated in equation 2, 3, and 4.

$$I_1=I_2 \qquad (2)$$

$$Z_{in}=\frac{[Z_O]^2}{2[R_L]} \qquad (3)$$

$$Z_{out}=2*R_L \qquad (4)$$

As we have seen from the equations above, the peaking class-C amplifier has DC quiescent current within the lower level of the threshold. This implies that from the principles of power amplifier theory, the class-C amplifier has higher efficiency with lower gain than the carrier class-AB amplifier. However, to have equal maximum output power between the carrier class-AB and peaking class-C amplifiers, the input power must be increased. This improves the overall performance of the two amplifiers, while amplitude modulation distortion will be eliminated [8].

III. THE DESIGN OF POWER AMPLIFIER

In this paper, the dynamic imbalanced load modulation approach has been demonstrated with design of class-AB as carrier amplifier and class-C as peaking amplifier, cascaded by the use of Si-LDMOS transistor model for 3.47-3.53 GHz. Theproposed design can provide more efficiency with dynamic range of linearity. The dynamic imbalanced load modulation adaptation is considered using transmission line impedance inverter of 50 ohms quarter wavelength. In the design of such power amplifier, there are steps that are essential to take into account, for high level performance of the entire design. The main thing to do in the design steps is to establish the DC characterization circuit. The DC simulation controls the bias point and bias network. This is based on the class of operation and power requirement. The bias condition was set for class-AB and class-C power amplifiers. The drain source voltage (VDS) for amplifier is 30 V each. The gate source voltage (VGS) for carrier amplifier is 3.0 V, while is 2.5 V for the peaking amplifier. Table 1 illustrates the DC simulation results for both carrier and peaking amplifiers.The DC simulation results state the class of operation. In the first stage, class-AB class of operation was selected and simulated before applying same process for class-C.

However, the design of bias network was based on class-AB and C RF power amplifiers. The maincause for good biasing is to guaranteepreclusion of signal reflection in the design. The DC quiescent current is realized to evade signal distortion effects. The radio frequency is prevented from reflecting back to the DC source[8]. On the matching network, the transistor input and output impedances are internally matched provided by the manufacturer.

An imbalanced splitter is designed as part of the dynamic load modulation RF power amplifier. In fact proper design of the splitter makes great impact to the total efficiency of the system. However, simulation testswere carried out to validate the design stability, insertion loss, the phase difference across the ports and isolation response of the splitter. Tests have also been carried in terms of operating frequency and bandwidthtestspresentedexcellenteffectson results. It should be noted that, the imbalanced splitter at the input split the input signal disproportionately between the carrier class-AB and peaking class-C amplifiers.An impedance transformer was used as imbalanced combinerbetween the outputs of the carrier class-AB, the peaking class-C. The impedance transformer is combined at the output to form a dynamic imbalanced load modulation RF power amplifier[8].

The dynamic imbalanced load modulation RF power amplifier was with RT 5880 substrates, Height of 0.5mm, relative permittivity of 2.2, T = 3 um and TanD = 0.017. This amplifier covers the range from 3.47 to 3.53GHz operating frequency, with acceptable return losses for input and output illustrated in figure 2.

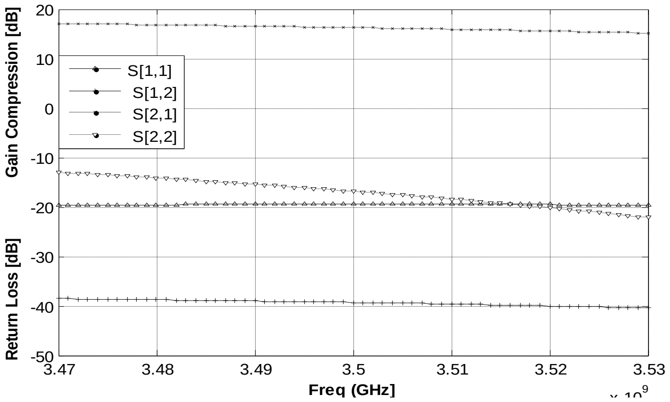

Figure 2:Linear simulation of the dynamic load modulation amplifier.

The simulation test performance results of dynamic imbalanced load modulation RF power amplifier in comparison with the balance power amplifier have been demonstrated. In the dynamic load modulation system, bias drain source voltage (VDS) for all transistors was chosen to be 30V, as shown in the data sheet. The bias gate source voltage (VGS) for carrier class-AB is 3.0V, while for class-C is 2.5V respectfully. The balance power amplifier (VGS) for both carrier and peaking amplifiers are given as 3.0V each. While (VDS) remain 30V obtained from the data sheet of the manufacturer. It is however essential to say due to the equal gate source voltage, the balance amplifier stability was more effective.

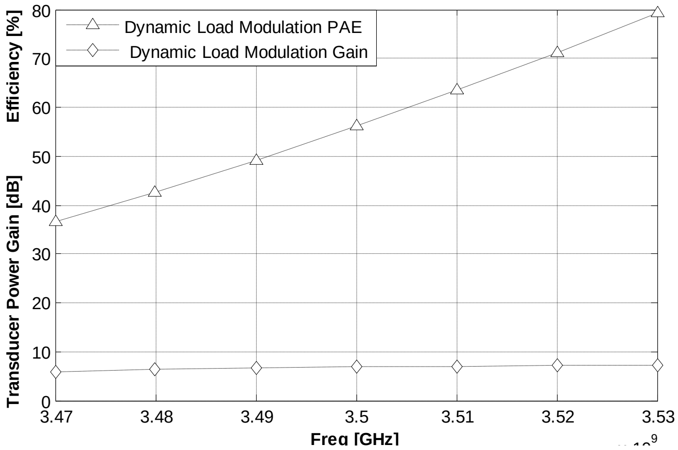

Figure 3:dynamic load modulation PAE and transducer power gain.

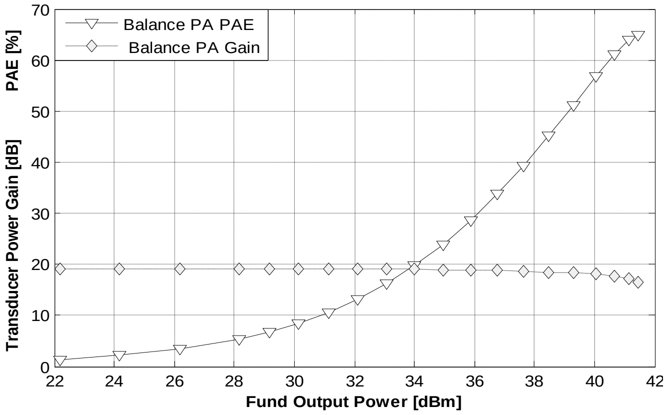

Figure III: Balance power amplifier PAE and transducer power gain.

Figure 3 and 4 characterized the power added efficiency as well as thetransducer power gain of the dynamic imbalanced load modulation RF power amplifier and that of balance power amplifier at 1dB compression point. The dynamic imbalanced load modulation RF power amplifier PAE = 79%, gain reduced to 8dB at pout = 35dBm. While, the balance power amplifier PAE = 65%, gain remain 19dB at pout = 41dBm. The performance of the dynamic imbalanced load modulation power amplifier has clearly indicated a massive increase in efficiency in less power against the balance power amplifier. So, this results of the have demonstrated a significant improvement from the design of the dynamic imbalanced load modulation power amplifier as illustrated in table 1.

Table 1:Performance comparison between dynamic load modulation and the balance power amplifier

System	Device	RF Range [GHz]	PAE [%]	P_{out} [dBm]	Gain [dB]
Dynamic Load Modulation	LDMOS	3.47-3.53	79	35	8
Balance Power Amplifier	LDMOS	3.47-3.53	65	41	19

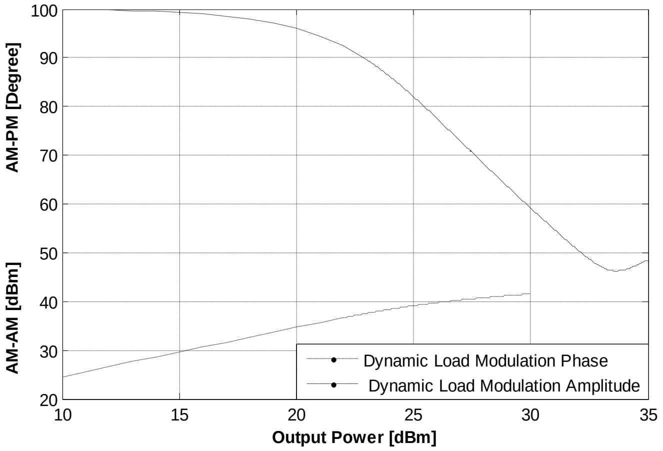

Figure 5: Dynamic load modulation AM-AM and AM-PM responses.

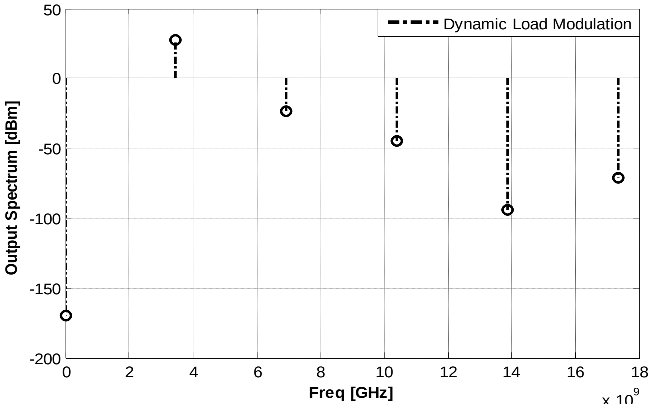

Figure 6: Fundamental frequency and harmonic components of the dynamic load modulation.

Figure 5 characterizedynamic imbalanced load modulation RF power amplifier AM-AM and AM-PM responses extracted from 1-tone test. Figure 6 also illustrates the output spectrum. The first frequency (3.5GHz) is the fundamental frequency with the various harmonic components.

IV. CONCLUSION

The work presented a new dynamic imbalance load modulation technique using an attenuator at the input of the carrier amplifier. The new dynamic imbalance load modulation technique is operating on class-AB and class-C amplifiers. However, the use of dynamic load modulation method causes excessive appreciation in PAE, drain efficiency and P_{out}.The dynamic load modulation technique is compared with balanced power amplifier technique to find a best candidate. A simulation results achieved from the dynamic load modulation power amplifier with 79% power added efficiency at 35dBm output power. The result has shown reasonable improve from dynamic load modulation over the balance power amplifier design.

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