

# Asymmetric Multilevel Inverter of 11-level Cascaded H-Bridge with Renewable Source connected to Grid

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#### -----ABSTRACT-----

In this world we have a huge demand for power with rapid development. As we have shortage of power we are implementing new techniques day by day to meet our daily demand. One of the best sources to meet our demands is to use renewable energy like large scale solar power plants. In our present paper we have come up with a new way of connecting photo-voltaic power plant (solar power plants) to main grids. Presently we are converting the output of solar power plants which is direct current into alternating currents by using high power rating inverters. In our modeling we are using multilevel H bridge cascaded inverters to get 11 level output. In our paper we are implementing asymmetric inputs of dc voltage sources (solar power plants) to inverters. We are going to replace a five level symmetric h bridge cascaded inverter (present system) with three level asymmetric h bridge cascaded inverters (proposed system). In this way we can further achieve high efficiency by reducing loses, number of switches and inverter size without any change in output of inverter.

#### Keywords - Multilevel Inverter cascaded H-bridges, PV arrays.

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|                                     | <br>                              |

# I. INTRODUCTION

Renewable energy is the future of world power demand. The form of renewable energy which is now becoming predominant and more employed is solar. Solar power plant comprises of set of many PV arrays connected together to get desired power. Solar energy is free and abundant in our nature. The solar power plant is also known as photo voltaic system or photo voltaic power plant. A grid-connected photovoltaic power system or grid-connected PV system is a generating p-v system which is connected to the utility grid. A gridconnected PV system consists of solar panels, one or several inverters, transformer, a power conditioning unit and grid connection equipment. Here the inverters are used to convert the dc output of the photo voltaic power system into alternating source as all the transmission and utilization systems are equipped with alternating current mechanism. They range from small residential and commercial rooftop systems to large utility-scale solar power stations. Unlike stand-alone power systems, a grid-connected system rarely includes an integrated battery solution, as they are still very expensive. When conditions are right, the grid-connected PV system supplies the excess power, beyond consumption by the connected load, to the utility grid. Further for this conversion of dc power to ac power we use different types of cascaded inverters. But the inverter produces square wave ac. The square wave contains infinite number of harmonics. So to reduce those harmonics we generally use multiple inverters and sum up all there outputs. Usually we use multiple inverters with same input magnitude and there output is added later. By using these better conversion techniques we can achieve better results and further improve implementation of green energy.

# II. PHOTO VOLTAIC ARRAY AND INVERTERS

### Photo voltaic system:

A photovoltaic system directly converts sunlight into electricity. The basic device of a PV system is the PV cell. Cells may be grouped to from panels or arrays. The voltage and current available at the terminals of a PV device may directly feed small loads such as lighting systems and DC motors. A photovoltaic cell is basically a semiconductor diode whose p-n junction is exposed to light. Photovoltaic cells are made of several types of semiconductors using different manufacturing processes. The incidence of light on the cell generates charge carriers that originate an electric current if the cell is short-circuited.



Fig.1 Equivalent circuit of PV device.

Fig.2 I-V Characteristic

### Inverters:

An Inverter is a simple electronic device which converts direct current into alternating current. An Inverter has a set of four transistors, IGBT or MOSFET and they are triggered simultaneously to achieve the sine wave. In actual case we won't get a sine wave instead we get a square wave. To achieve a pure sine wave we use several filter circuits. We also use multi-level inverters to get a pure form of sine wave. In the figure below we can see two types of wave forms. The wave form on the left side (a) is a pure sinusoidal wave form where as the wave form on the right side (b) is the alternating current waveform which is achieved by using a simple inverter.



Figure 3: pure sine wave and square wave

# **III. CASCADED H BRIDGE INVERTERS**

The H bridge inverters are type of inverters which allows the flow of current in all directions. The H ridge inverter which we are using has four IGBT's which are connected in the form of a bridge. Several H bridge inverters are connected to each other in series form and this is known as series cascading. We do this series cascading in order to obtain the output as the sum of all H Bridge inverters. In our paper we have two different forms of series cascaded H Bridge inverters. They are five bridge cascaded symmetric inverter which has five inverters connected to each other by series cascading and the other is three level cascaded asymmetric inverter which has three bridges connected to each other by series cascading. In both the cases we are giving dc voltage as input and we obtaining 11 level sinusoidal outputs. In our current paper discussion we are going to see in detail about both the inverters with their working in detail and there components.

# Eleven level output wave form:



# SYMMETRIC MODEL (OR) EXISTING SYSTEM:

The existing system, 11-level CHB MLI has 5 H-bridge inverters. The number of voltage levels in the output voltage by using the equation is (2n+1), the 'n' means one full H-bridge inverter. One full H-bridge inverter have 4 switches. The numbers of switches in 11-level CHB MLI are 20 switches and additional 4 switches are used for power continuity. In this 11 level CHB MLI is operated with switching frequency is high (carrier frequency). The level shift phase dispose Pulse Width Modulation (PWM) Technique are used. In symmetrical multilevel inverter, all H-bridge cells are fed by equal voltages, and hence all the arm cells produce similar output voltage steps. However, if all the cells are not fed by equal voltages, the inverter becomes an asymmetrical one. In this inverter, the arm cells have different effect on the output voltage. Other topologies are possible, such as the neutral point clamped fed by unequal capacitors





In this symmetric five Bridge model we have five bridges and 25 switches connected to each other by series cascading. The input to each inverter is given from PV array. In our block diagram representation we are representing PV sources as dc voltage sources. The input voltage to each inverter in the model is equal in symmetric model and let it be (v1=v2=v3=v4=v5=45v). As we use five inverter bridges and we give 45 volts to each bridge we get  $(45\times5=230v)$  output when we add them.

# TRIGGERTING SEQUENCE OF SWITCHES: (EXISTING SYSTEM)

In existing model we are having switches Q1 to Q20 for five brides in inverters and extra switches Q21 to Q25 for achieving continuity of power. When the switch is in on position it is represented by 1 and when switch is in off position it is represented by 0.

| ¥ |                |                       |                |    |    |    |    | -                     |                |        |                 | -       |                 |                 | -               |                 |                 |                        |                 |     |                 |                 |                 |                 |                 |                 |
|---|----------------|-----------------------|----------------|----|----|----|----|-----------------------|----------------|--------|-----------------|---------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|-----------------|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
|   |                |                       |                |    |    |    |    | Sw                    | itchi          | ng seo | quenc           | es of S | Single          | Phase           | e Sym           | metric          | e 11-le         | evel C                 | HB M            | ILI |                 |                 |                 |                 |                 |                 |
|   |                |                       |                |    |    |    |    |                       |                |        |                 |         |                 |                 |                 |                 |                 |                        |                 |     |                 |                 |                 |                 |                 |                 |
|   | V <sub>s</sub> | <b>Q</b> <sub>1</sub> | Q <sub>2</sub> | Q3 | Q4 | Q₅ | Qő | <b>Q</b> <sub>7</sub> | Q <sub>8</sub> | Q۹     | Q <sub>10</sub> | Q11     | Q <sub>12</sub> | Q <sub>13</sub> | Q <sub>14</sub> | Q <sub>15</sub> | Q <sub>16</sub> | <b>Q</b> <sub>17</sub> | Q <sub>18</sub> | Q19 | Q <sub>20</sub> | Q <sub>21</sub> | Q <sub>22</sub> | Q <sub>23</sub> | Q <sub>24</sub> | Q <sub>25</sub> |
|   | 5v             | 1                     | 1              | 0  | 0  | 1  | 1  | 0                     | 0              | 1      | 1               | 0       | 0               | 1               | 1               | 0               | 0               | 1                      | 1               | 0   | 0               | 0               | 0               | 0               | 0               | 0               |
| 4 | 4v             | 1                     | 1              | 0  | 0  | 1  | 1  | 0                     | 0              | 1      | 1               | 0       | 0               | 1               | 1               | 0               | 0               | 0                      | 0               | 0   | 0               | 0               | 0               | 0               | 0               | 1               |
|   | 3v             | 1                     | 1              | 0  | 0  | 1  | 1  | 0                     | 0              | 1      | 1               | 0       | 0               | 0               | 0               | 0               | 0               | 0                      | 0               | 0   | 0               | 0               | 0               | 0               | 1               | 1               |
|   | 2v             | 1                     | 1              | 0  | 0  | 1  | 1  | 0                     | 0              | 0      | 0               | 0       | 0               | 0               | 0               | 0               | 0               | 0                      | 0               | 0   | 0               | 0               | 0               | 1               | 1               | 1               |
|   | 1v             | 1                     | 1              | 0  | 0  | 0  | 0  | 0                     | 0              | 0      | 0               | 0       | 0               | 0               | 0               | 0               | 0               | 0                      | 0               | 0   | 0               | 0               | 1               | 1               | 1               | 1               |
| ( | 0              | 0                     | 0              | 0  | 0  | 0  | 0  | 0                     | 0              | 0      | 0               | 0       | 0               | 0               | 0               | 0               | 0               | 0                      | 0               | 0   | 0               | 1               | 1               | 1               | 1               | 1               |
|   | -1v            | 0                     | 0              | 1  | 1  | 0  | 0  | 0                     | 0              | 0      | 0               | 0       | 0               | 0               | 0               | 0               | 0               | 0                      | 0               | 0   | 0               | 0               | 1               | 1               | 1               | 1               |
|   | -2v            | 0                     | 0              | 1  | 1  | 0  | 0  | 1                     | 1              | 0      | 0               | 0       | 0               | 0               | 0               | 0               | 0               | 0                      | 0               | 0   | 0               | 0               | 0               | 1               | 1               | 1               |
|   | -3v            | 0                     | 0              | 1  | 1  | 0  | 0  | 1                     | 1              | 0      | 0               | 1       | 1               | 0               | 0               | 0               | 0               | 0                      | 0               | 0   | 0               | 0               | 0               | 0               | 1               | 1               |
|   | -4v            | 0                     | 0              | 1  | 1  | 0  | 0  | 1                     | 1              | 0      | 0               | 1       | 1               | 0               | 0               | 1               | 1               | 0                      | 0               | 0   | 0               | 0               | 0               | 0               | 0               | 1               |
|   | -5v            | 0                     | 0              | 1  | 1  | 0  | 0  | 1                     | 1              | 0      | 0               | 1       | 1               | 0               | 0               | 1               | 1               | 0                      | 0               | 1   | 1               | 0               | 0               | 0               | 0               | 0               |

Asymmetric Multilevel Inverter of 11-level Cascaded ...

ELEVEN LEVEL CASCADED H-BRIDGE MULTI LEVEL INVERTER OUTPUT:



FIGURE: 6 CASCADED H BRIDGE MLI FOR ELEVEN LEVELS.

# ASYMMETRIC MODEL OR PROPOSED SYSTEM:

Proposed system has Asymmetric 11-level CHB MLI has only 12 switches and 3 additional switches for the continuity of power. The switches are operated with switching frequency is low (fundamental frequency). In this newly proposed Asymmetric 11-level CHB MLI has advantages compared to the existing system are number of switches, switching losses, control circuit and also size of the circuit reduces. The proposed system of Asymmetrical 11-level CHB MLI with their input sources are PV arrays connected to grid. Asymmetrical multilevel inverter has been recently investigated. In all these studies, H-bridge topology has been considered and a variety of selections of cascaded cell numbers and dc-sources ratios have been adopted. The suggested pulse width-modulation strategy that maintains the high-voltage stage to operate at low frequency limits the source-voltage selection. It can optimize the number of output levels (any odd number from 2K+1 to 3K), by using H-bridges scaled in power of three, without increasing the number of converters. The corresponding "Asymmetrical" topology provides more flexibility to the designer



Figure: 6 proposed model of 3 level cascaded h bridge inverter

In this asymmetric modeling of the three bridge inverter the input voltages are not equal let them be v1, v2 and v3. We have taken that v1=v2=46v and v3= 138v. And correspondingly to obtain different levels different switches are triggered. The triggering sequence is showed below.

# TRIGGERTING SEQUENCE OF SWITCHES: (PROPOSED SYSTEM):

In our proposed model we have fifteen switches in total where switches Q1 to Q12 are for inverters of three level cascaded and the switches Q13, Q14 and Q15 are to achieve continuity of the new system. The corresponding "Asymmetrical" topology provides more flexibility.

|            | Sv                    | vitch                 | ing s          | eque                  | nces | of Si                 | ingle                 | Pha                   | se As | ymme            | etric 11        | l-level         | CHB N           | ALI             |                 |
|------------|-----------------------|-----------------------|----------------|-----------------------|------|-----------------------|-----------------------|-----------------------|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Vs         | <b>Q</b> <sub>1</sub> | <b>Q</b> <sub>2</sub> | Q <sub>3</sub> | <b>Q</b> <sub>4</sub> | Q5   | <b>Q</b> <sub>6</sub> | <b>Q</b> <sub>7</sub> | <b>Q</b> <sub>8</sub> | Q9    | Q <sub>10</sub> | Q <sub>11</sub> | Q <sub>12</sub> | Q <sub>13</sub> | Q <sub>14</sub> | Q <sub>15</sub> |
| 5v         | 1                     | 1                     | 0              | 0                     | 1    | 1                     | 0                     | 0                     | 1     | 1               | 0               | 0               | 0               | 0               | 0               |
| <b>4</b> v | 1                     | 1                     | 0              | 0                     | 0    | 0                     | 0                     | 0                     | 1     | 1               | 0               | 0               | 0               | 1               | 0               |
| 3v         | 0                     | 0                     | 0              | 0                     | 0    | 0                     | 0                     | 0                     | 1     | 1               | 0               | 0               | 1               | 1               | 0               |
| 2v         | 1                     | 1                     | 0              | 0                     | 1    | 1                     | 0                     | 0                     | 0     | 0               | 0               | 0               | 0               | 0               | 1               |
| 1v         | 1                     | 1                     | 0              | 0                     | 0    | 0                     | 0                     | 0                     | 0     | 0               | 0               | 0               | 0               | 1               | 1               |
| 0v         | 0                     | 0                     | 0              | 0                     | 0    | 0                     | 0                     | 0                     | 0     | 0               | 0               | 0               | 1               | 1               | 1               |
| -1v        | 0                     | 0                     | 1              | 1                     | 0    | 0                     | 0                     | 0                     | 0     | 0               | 0               | 0               | 0               | 1               | 1               |
| -2v        | 0                     | 0                     | 1              | 1                     | 0    | 0                     | 1                     | 1                     | 0     | 0               | 0               | 0               | 0               | 0               | 1               |
| -3v        | 0                     | 0                     | 0              | 0                     | 0    | 0                     | 0                     | 0                     | 0     | 0               | 1               | 1               | 1               | 1               | 0               |
| -4v        | 0                     | 0                     | 1              | 1                     | 0    | 0                     | 0                     | 0                     | 0     | 0               | 1               | 1               | 0               | 1               | 0               |
| -5v        | 0                     | 0                     | 1              | 1                     | 0    | 0                     | 1                     | 1                     | 0     | 0               | 1               | 1               | 0               | 0               | 0               |

# COMPARISION BETWEEN TWO SYSTEMS:

In our first system we have five inverters where as in our second system we have three inverters. In our first system we have a total 25 switches where as in our second system we have 15 switches. We give symmetric input voltages to the first system where as in second system we give asymmetric voltage sources.

Input voltage levels of two systems:

| Voltage ratings | Existing system | Proposed system |
|-----------------|-----------------|-----------------|
| (volts)         | (volts)         | (volts)         |
| V <sub>1</sub>  | 46              | 46              |
| $V_2$           | 46              | 46              |
| V <sub>3</sub>  | 46              | 138             |
| $V_4$           | 46              | -               |
| V <sub>5</sub>  | 46              | -               |

### Main Differences between two systems:

| Existing system                         | Proposed system                         |
|---|---|
| 1.Number of switches are                | 1. Number of switches are               |
| high                                    | less                                    |
| 2.size of the inverter circuit is       | 2. size of the inverter circuit         |
| more                                    | is less                                 |
| 3. switches are operated with           | 3. switches are operated with           |
| high frequency                          | fundamental frequency                   |
| 4.Switching losses are more             | 4. Switching losses are less            |
| 5. control circuit is difficult         | 5.control circuit is easy               |
| 6.Protection circuit                    | 6. Protection circuit                   |
| equipment is high                       | equipment is less                       |
| 7. Cooling equipment is high            | 7. Cooling equipment is less            |
| 8. Cost of the inverter circuit is more | 8. Cost of the inverter circuit is less |

#### **IV.** CONCLUSION

1. This paper presents an 11-level CHB MLI, which optimizes the existing system by the proposed system. The system input voltages are taken as PV arrays and connected to the grid system.

2. The advantage of the proposed system is that there is a reduction in switching losses due to reduction in number of switches. This also decreases the complexity of the circuit.

In this way the size of the inverter, number of switches, and heating losses have been reduced and further the efficiency of the inverter have been increased.

The only limitation which we have in proposed system is that we have increased the power rating of one switch.

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