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DESIGN AND ANALYSIS OF A 4-BIT LOW POWER BARREL SHIFTER IN 20nm FINFET TECHNOLOGY

[1,]Rinu Pappachan, [2,]V.Vijayakumar, [3,]T.Ravi, [4,]V.Kannan
[1,]*M.Tech-VLSI Design, Sathyabama University, Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai 119*
[2,3,]*Assistant Professor, Sathyabama University, Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai 119.*
[4,]*Principal, Jeppiaar Institute Of Technology, Kunnam, Tamilnadu, India.*

----------Abstract----------
A barrel shifter is an important block of a floating point arithmetic unit and it is capable of shifting data word by a specified 'n' number of bits in one cycle. Whereas shift registers are capable of shifting only one bit in one clock cycle. Barrel shifter can perform the following functions: shift left logical, shift left arithmetic, rotate left, shift right logical, shift right arithmetic and rotate right. The design of the barrel shifter is purely MUX based and therefore designing a MUX for low power to use it as a repetitive block in the barrel shifter will improve its efficiency. The MUX based barrel shifter circuits are designed using transmission gate. The barrel shifter is designed in FinFET technology. Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS in nano-scale circuits.

Keywords *– barrel shifter, low power, MUX, shifting, rotating*

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I. Introduction

Barrel shifters are used for shifting and rotating data which is required in several applications like floating point adders, variable-length coding, and bit-indexing. Barrel shifters, are commonly found in both digital signal processors and general-purpose processors. The MUX based barrel shifter architecture are designed using 4:1, 8:1, 16:1, 32:1 and 64:1 MUX trees. Each MUX tree is designed using 2:1 MUX as the basic building block[1]. The power consumed by MUX trees is quite significant and cannot be ignored. Thus, it is important to minimize power dissipation of MUX trees within low-power designs.Multiplexers are digital circuit that generates an output that exactly reflects state of one of a number of data inputs, based on value of select lines is. A multiplexer with two data inputs and one select line is referred as "2-to-1 or2:1" multiplexer.

FinFETs are double-gate transistors in which the two gates can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. For FinFET there are three modes of operation namely, the shorted-gate (SG) mode with transistor gates tied together, the low-power (LP) mode where the back-gate is tied to a reverse-bias voltage to reduce leakage power, and the independent gate (IG) mode where independent digital signals are used to drive the two device gates.[18]

II. 4-Bit Mux Based Barrel Shifter Architecture Design

The behavior of 4-bit MUX based barrel shifter are shown in table 1 which has the following control signals:- D controls the direction, S/R for shift/rotate operation, L/A for logical/arithmetic shift and S1,S0 for number of bits to be shifted or rotated. I0,I1,I2,I3 and Y0.Y1,Y2,Y3 represents the input bits and output bits respectively. The circuit can be used to rotate or shift a 4-bit word in both right and left direction by 0,1,2,3 bits. D='0' means the direction of shift/rotate operation is towards right and D='1' means it is towards left. The control signal S/R='0' represents shift operation and S/R='1' represents rotate operation. When L/A=''0' it is logical shift, L/A='1' it is arithmetic shift and when L/A='x' it is rotate operation. The bits S1, S0 are length selection bits. S1S0='00' means the length is 0 bit, S1S0='01' means the length is 1 bit, SIS0='10'means the length is 2 bits, S1S0='11' means the length is 3 bits. Table 1 explains the various operations performed by 4-bit barrel shifter. As there are five control signals, we need a 32:1 MUX for each output bit. Thus for 4 output bits, we need four 32:1 MUX in the design of a 4-bit barrel shifter. Each column of truth table can be implemented with a dedicated 32:1 MUX circuit, which is designed using 2:1 MUX cell, to obtain final output [1]. Logical shift is a bitwise operation that shifts all the bits of its operand. The two logic shift operations are the logical left shift and the logical right shift. Unlike an arithmetic shift, a logical shift does not preserve a number's sign bit that is the MSB. Logical shifts are equivalent to performing multiplication or division of

unsigned integers by powers of two. Logical right shift by 'n' bits have the same effect of multiplying it by 2^n and logical left shift by 'n' bits will have the same effect of dividing it by 2^n.The 8X1 MUX and 4X4 barrel shifter is designed using FinFET in shorted gate(SG) mode.

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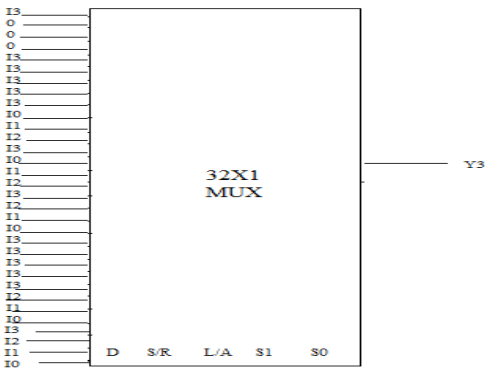
(a) (b)

FIG.1. (A) SG P-FINFET (B) SG N-FINFET

Table 1. Truth-Table for 4-bit barrel shifter

OPERATION	**D**	**S/R**	**L/A**	**S1**	**S0**	**Y3**	**Y2**	**Y1**	**Y0**
SHIFT RIGHT LOGICAL	0	0	0	0	0	I3	I2	I1	I0
	0	0	0	0	1	0	I3	I2	I1
	0	0	0	1	0	0	0	I3	I2
	0	0	0	1	1	0	0	0	I3
SHIFT RIGHT ARITHMETIC	0	0	1	0	0	I3	I2	I1	I0
	0	0	1	0	1	I3	I3	I2	I1
	0	0	1	1	0	I3	I3	I3	I2
	0	0	1	1	1	I3	I3	I3	I3
ROTATE RIGHT	0	1	X	0	0	I3	I2	I1	I0
	0	1	X	0	1	I0	I3	I2	I1
	0	1	X	1	0	I1	I0	I3	I2
	0	1	X	1	1	I2	I1	I0	I3
SHIFT LEFT LOGICAL	1	0	0	0	0	I3	I2	I1	I0
	1	0	0	0	1	I2	I1	I0	0
	1	0	0	1	0	I1	I0	0	0
	1	0	0	1	1	I0	0	0	0
OPERATION	**D**	**S/R**	**L/A**	**S1**	**S0**	**Y3**	**Y2**	**Y1**	**Y0**
SHIFT LEFT ARITHMETIC	1	0	1	0	0	I3	I2	I1	I0
	1	0	1	0	1	I3	I1	I0	0
	1	0	1	1	0	I3	I0	0	0
	1	0	1	1	1	I3	0	0	0
ROTATE LEFT	1	1	X	0	0	I3	I2	I1	I0
	1	1	X	0	1	I2	I1	I0	I3
	1	1	X	1	0	I1	I0	I3	I2
	1	1	X	1	1	I0	I3	I2	I1



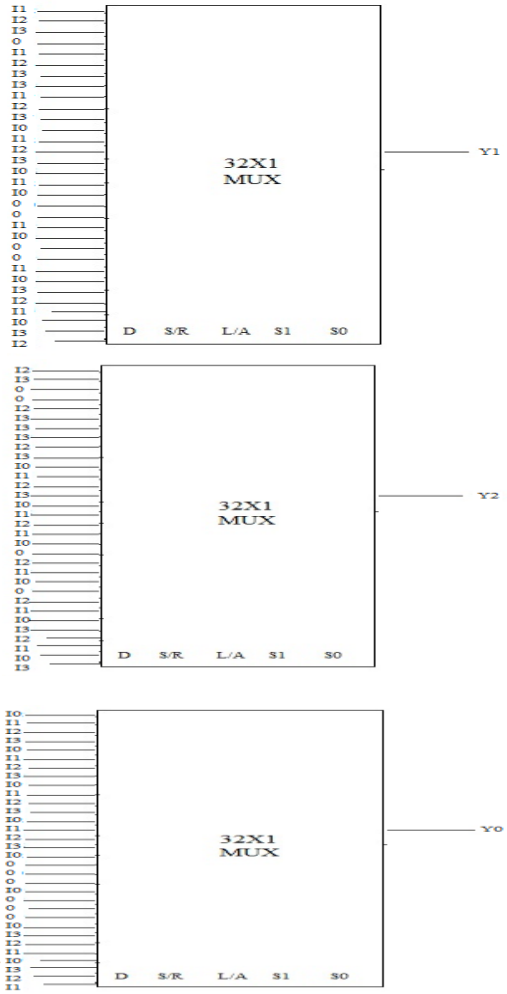


FIG.2. ARCHITECTURE OF A 4-BIT BARREL SHIFTER

2.1 FinFET

The power consumption in battery-operated portable devices is a major concern. Even for nonportable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (very-large-scale integration) designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increased importance. FinFETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (complementary metal-oxide-semiconductor) at 22-nm and beyond, offer interesting delay–power tradeoffs. Both CMOS logic and pass transistor logic were developed for conventional NMOS and PMOS transistor. In FinFET the NMOS in CMOS technology is replaced with NFinFET and PMOS with PFinFET, then, both gates of FinFET are tied together. By using this approach, we can design a FinFET version of a CMOS logic circuit or a pass transistor logic circuit that retains the same functionalities as the MOSFET version. In the mean time, FinFET provides better circuit performances and reduces leakage current through effective suppression of short-channel effect and near-ideal subthreshold swing.[18]

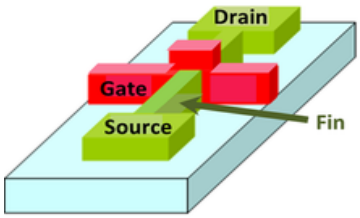


FIG.3. FINFET STRUCTURE[19]

Double-gate (DG) FinFETs are broadly classified into two types, namely, simultaneously driven double-gate (SDDG) and independently driven double gate (IDDG) FinFETs. SDDG behaves like a three-terminal MOSFET because it has both the gates (front and back) connected each other, whereas the IDDG has two independent gates.In conventional MUX tree the MSB of selection input, S2 is given to the level 2 and LSB of selection input, S0 is given to the level 0. Here the switching activity of MUXes in MUX tree is more because S0 is having higher frequency. So when S0 is switched the four MUXes in level 0 is switched.

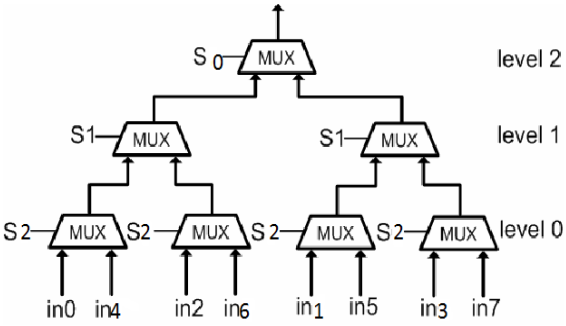


FIG.5. PROPOSED ARCHITECTURE OF 8X1 MUX

In proposed MUX tree the MSB of selection input (S2) is given to the level 0 and LSB of selection input (S0) is given to the level 2. Here the switching activity of MUXes in MUX tree is less when compared to the conventional MUX tree because S2 is having lower frequency and is given to level 0 which has the large number of MUXes. So when S0 is switched only one MUX in level 2 is switched. Since the switching activity is less in proposed MUX when compared with the existing MUX the power will also be less in proposed MUX. This proposed MUX is used to design the proposed 4-bit barrel shifter.

2.2 MUX Decomposition

The problem of MUX decomposition is that of converting an n-to-1 MUX into logically equivalent MUX tree of 2-to-1 MUXes. There are various arrangements possible to build. But for power optimization it is required to use the proper MUX structure to do so.

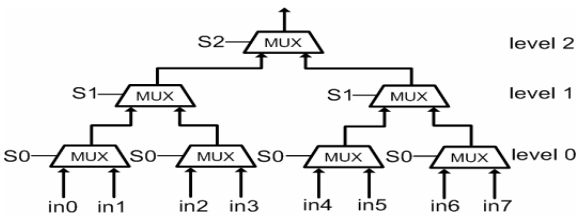


FIG.4. CONVENTIONAL ARCHITECTURE OF 8X1 MUX [11]

III. Result And Discussion

The designs are simulated in HSPICE using 20nm FinFET technology. The fig 6 and 7 shows the transient analysis of existing 8X1 MUX and existing 4x4 barrel shifter. The fig 8 and 9 shows the transient analysis of proposed 8X1 MUX and proposed 4X4 barrel shifter. Table 2 and 3 shows the performance of 8:1 MUX, 4x4 barrel shifter.

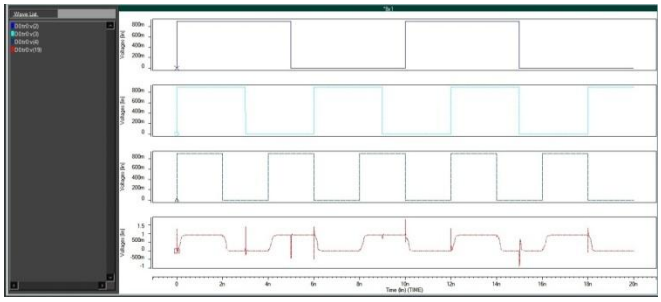


FIG.6. SIMULATION OUTPUT OF EXISTING 8X1 MUX

- v(2),v(3) and v(4) are the selection lines and
- v(19) is the output for the input 10101010.

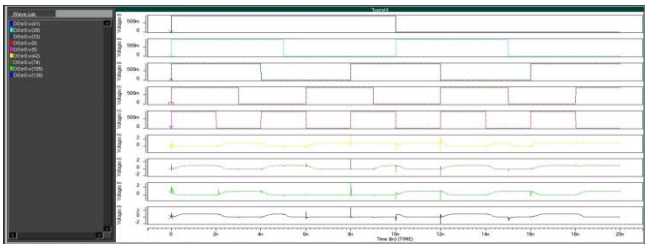


FIG.7. SIMULATION OUTPUT OF EXISTING 4X4 BARREL SHIFTER

- v(41),v(38) and v(33) are the selection line for choosing which operation to be performed.
- V(8) and v(5) are selection line for choosing number of bits to be shifted and
- v(42),v(74) and
- v(105),v(136) are the outputs for the input 1010.

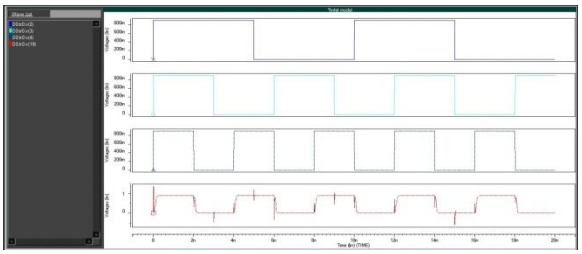


FIG.8. SIMULATION OUTPUT OF PROPOSED 8X1 MUX

- v(2),v(3) and v(4) are the selection lines and
- v(19) is the output for the input 10101010.

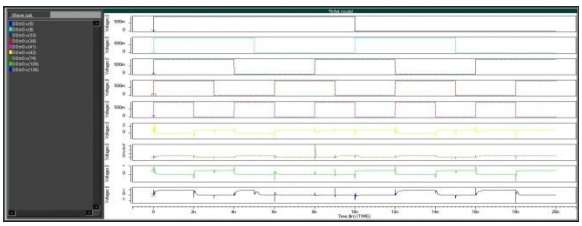


FIG.9. SIMULATION OUTPUT PROPOSED OF 4X4 BARREL SHIFTER

- v(41),v(38) and v(33) are the selection line for choosing which operation to be performed.
- V(8) and v(5) are selection line for choosing number of bits to be shifted and
- v(42),v(74) and
- v(105),v(136) are the outputs for the input 1010.

Table 2. Performance analysis of MUX in 130nm MOSFET technology

Architecture design	Avg.power (W)	Delay (S)	PDP (J)
Existing 8X1 MUX	1.318e-04	45e-12	59.31e-16
Proposed 8X1 MUX	5.199e-05	23e-12	11.95e-16

Table 3. Performance analysis of 4 –bit barrel shifter using 130nm MOSFET technology

Architecture design	Avg.power (W)	Delay (S)	PDP (J)
Existing 4X4 barrel shifter	1.760e-03	67.8e-12	11.93e-14
Proposed 4X4 barrel shifter	0.412e-03	28.34e-12	1.16e-14

Table 4. Performance analysis of MUX in 32nm MOSFET technology

Architecture design	Avg.power (W)	Delay (S)	PDP (J)
Existing 8X1 MUX	3.800E-05	22.1e-12	83.98e-17
Proposed 8X1 MUX	0.260e-05	13.4e-12	3.49e-17

Table 5. Performance analysis of 4 –bit barrel shifter using 32nm MOSFET technology

Architecture design	Avg.power (W)	Delay (S)	PDP (J)
Existing 4X4 barrel shifter	3.047e-06	40.4e-12	12.3e-17
Proposed 4X4 barrel shifter	0.845e-06	10e-12	0.845e-17

Table 6. Performance analysis of MUX in 20nm FinFET technology

Architecture design	Avg.power (W)	Delay (S)	PDP (J)
Existing 8X1 MUX	1.205e-07	19e-12	22.89e-19
Proposed 8X1 MUX	4.931e-08	7.5e-12	3.69e-19

Table 7. Performance analysis of 4-bit barrel shifter in 20nm FinFET technology

Architecture design	Avg.power (W)	Delay (S)	PDP (J)
Existing 4X4 barrel shifter	4.650e-04	53.84e-12	25.03e-15
Proposed 4X4 barrel shifter	1.137e-04	19.8e-12	2.25e-15

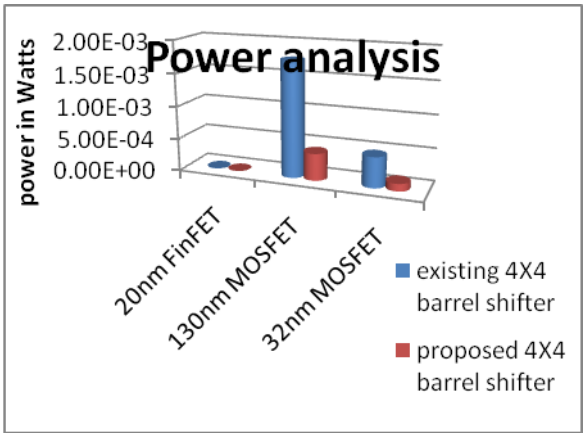


Chart1. Power analysis of 4X4 barrel shifter in different technologies

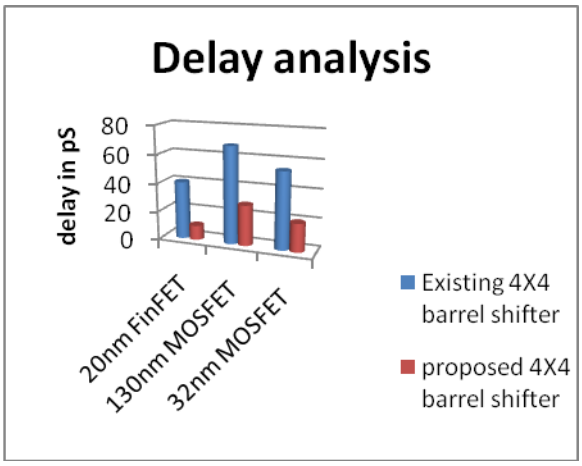


Chart2. Delay analysis of 4X4 barrel shifter in different technologies

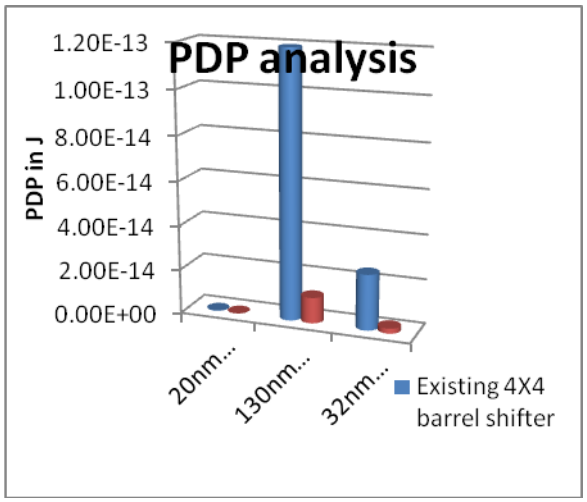


Chart3. PDP analysis of 4X4 barrel shifter in different technologies

IV. Conclusion

Barrel shifter can be designed using combinational logic circuits such as multiplexers, decoders and logic gates. A purely MUX based barrel shifter will have less power and delay when compared to other architectures. The barrel shifter is designed using the proposed MUX based architecture, reduces the power consumption. The existing system and proposed system is designed using 20nm FinFET technology. It is clear from fig 10, 11 and 12 the power, delay and PDP is much more improved for FinFET.

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Rinu Pappachan was born in Thiruvanathapuram, Kerala, 16th July 1988. She received her Bachelor Degree in Electronics and Communication Engineering, from Cochin University, Trivandrum, Kerala in the year 2010. M.TECH., VLSI DESIGN, Sathyabama University, Chennai, Tamilnadu, India.

V.Vijayakumar was born in Tiruvarur, Tamilnadu, India in 1983. He received his Bachelor Degree in Physics from Bharathidasan University in the year 2003, Master Degree in Physics from Bharathidasan University in the year 2006. Master Degree in VLSI DESIGN from Sathyabama University in the year 2008. Currently he is doing Ph.D in Sathyabama University. He is working as Assistant Professor in Department of ECE in Sathyabama University. His interested areas of research are Nano Electronics, VLSI Design, He has Research publications in National / International Journals / Conferences.

T.Ravi was born in Namakkal, Tamilnadu, India in 1978. He received his Bachelor Degree in Electrical and Electronics Engineering from Madurai Kamaraj University in the year 2001, Master Degree in Applied Electronics from Sathyabama Deemed University in the year 2004. Currently he is doing Ph.D in Sathyabama University. He is working as Assistant Professor in Department of ECE in Sathyabama University. His interested areas of research are Nano Electronics, VLSI Design, Low Power VLSI Design and Mixed Signal circuits. He has Research publications in National / International Journals /Conferences. He is a member of VLSI Society of India.

Dr.V.Kannan was born in Ariyalore, Tamilnadu, India in 1970. He received his Bachelor Degree in Electronics and Communication Engineering from Madurai Kamaraj University in the year 1991, Master Degree in Electronics and control from BITS, Pilani in the year 1996 and Ph.D., from Sathyabama University, Chennai, in the year 2006. His interested areas of research are Optoelectronic Devices ,VLSI Design, Nano Electronics, Digital Signal Processing and Image Processing. He has 150 Research publications in National / International Journals / Conferences to his credit. He has 21 years of experience in teaching and presently working as Principal, Jeppiaar Institute of Technology, Kunnam, Tamilnadu, India. He is a life member of ISTE.