The International Journal Of Engineering And Science (IJES)
ISSN (e): 2319 – 1813 ISSN (p): 2319 – 1805
Pages || 75- 79|| March - 2015 ||

Design and development of fully automated acaja5 card tester

C.Dhamotharan[1], P.Prabhu[2]
1. Assistant professor, 2.Assistant professor
Department of Electronics and Communication
RVS College of Engineering and Technology

----------**ABSTRACT**----------
OCB283 is a versatile digital switching system designed to meet all types of modern communication needs. The system has novel features like automatic recovery and double remoting. Due to these features and because of existing E10B system, the system is especially suitable for Indian network. OCB283 is a system which contains many PCBs for different functions involved in a telephone exchange. The ACAJA5 card is the internal ring communication controller based on token ring protocol. The aim of our project is to check the memory section of the card using program in Visual Basic6.0 by interfacing the card to the PC. To achieve this we have to interface the card with PC using an interface circuit. This interface card is connected with PC through Enhanced Parallel Port. Software is developed using Visual Basic to achieve our aim. This project will enable us to have an easy mechanism of automatically testing the ACAJA5 card instead of the older method using rack system

KEYWORDS- *OCB283, ACAJA5 card, Enhanced Parallel Port, Visual Basic6.0.*

I. INTRODUCTION

The telephone that seems easily available to us actually works through a complex method of switching and distribution. The process entered this area to simplify switching and thus replacing manually operated switches. The OCB283 telephone exchange is the latest one makes use of MOTOROLA 68000 series processor as the main processor, has a very high speed of switching and supports thousands of lines while occupying a relatively small space.

OCB283 is a digital switching system, developed by CIT ALCATEL of France, supports a variety of communication needs like basic telephony, ISDN, mobile communication, data communication etc. With all these hi-tech services that could be integrated by a single exchange, need for error handling become of utmost importance. The various stages of manufacturing, integration and customer servicing employs hundreds of cards. Testing of these various cards manually using CRO is a cumbersome task. Employing a PC for this purpose make a more efficient system. This project attempts to increase the testing efficiency of the ACAJA5 card used in OCB283 exchange. An interface card is designed and software program is developed to test a RAM in ACAJA5 card.

ACAJA5 card is used in OCB283 exchange as Token Ring Coupler. It has a function of interconnecting the racks in the OCB283 through a token Ring A and controlling the communication through it. It has an independent microprocessor, RAM, ROM etc. A card called ACAJB5 is also used in OCB283 which is responsible for controlling Token Ring B which is used in emergency.

Our project aim is to test the memory portions available in ACAJA5. Here we use software to control testing. Here we are using the parallel port of the PC to write and read data from the ACAJA5 card. As the parallel port has only limited number of pins for data input and output, we have to use an interface card so that communication between the ACAJA5 card and PC can take place. EPP mode is used because it is very easy to program.

II. IDEA OF THE PROJECT

Here we use the software to control the testing. The parallel port of the pc is used to write and read from the board. As the parallel port has only limited number of pins (8 pins) for data input and output, we have to use interface card so that communication between the ACAJA5 and PC can takes place.

EPP mode of the parallel port is used to transmit and receive data since it is very easy to program.The interface card consists of latches, controller and buffers. Its main function is to interconnect PC with the ACAJA5 card.

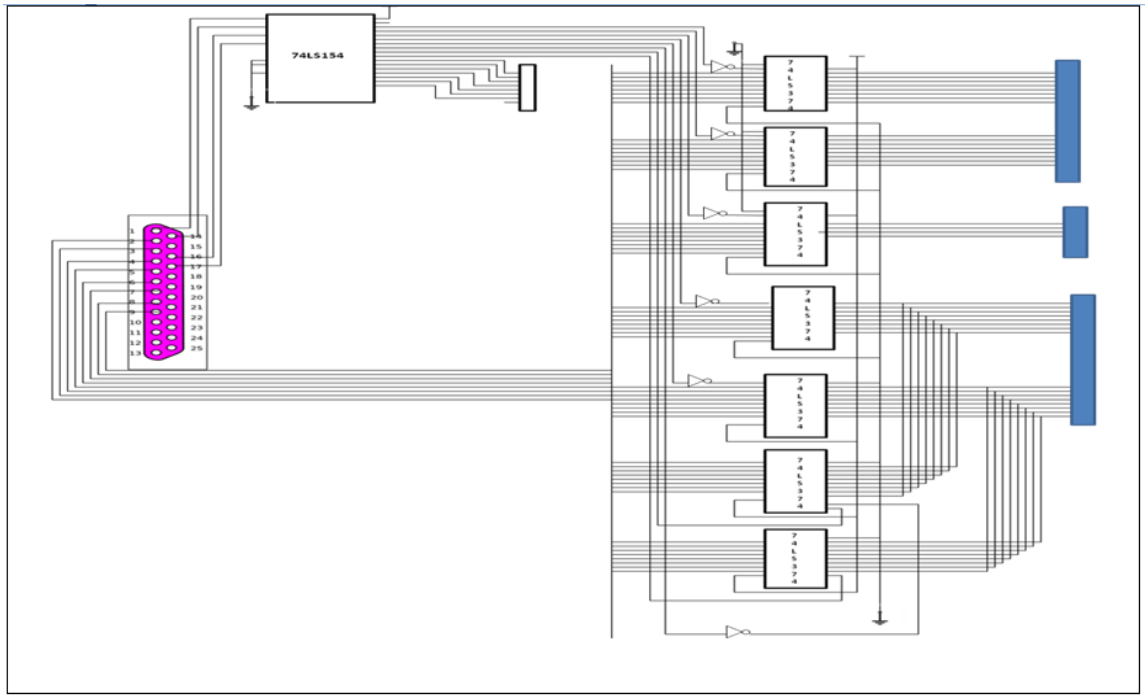
In this project, we are checking the status of the four static RAM (SRAM) in the ACAJA5 card. At first we check the state of the 20 address pins of the RAMs. The 20 address pins are common to all 4 RAMs. We check whether the pins are short using parallel port of the PC and software in VB. Secondly, we check whether the RAM can be written and read. For this we first write data to the RAM using parallel port of the PC and software. This data written is stored in a file. Then we read the data that was written to the RAM using parallel port of the PC and software. This data is stored in another file. Then these two files are compared and analyzed to find out the error in the locations of the RAM

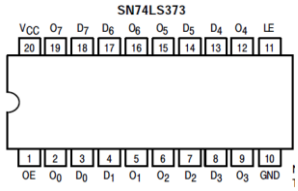
III. ARCHITECTURAL DETAILS

In this circuit we use latches (74LS374), controllers and demultiplexers (74LS138). Here the flip-flops are in high impedance state until they are enabled. On enabling the flip-flop, the values at their input are available at the output. Latches have the previous value until they are enabled. When latches are enabled, the present value is available at output and when they are disabled, the last value at the input latched at the output.
The simplicity and ease of programming makes the parallel port popular.EPP is more commonly used because it generate and control all the transfers to and from the peripherel.The control lines of parallel port are connected to the demultiplexer.The data is given retrieved from the data pins of the parallel port.The address to the RAM is given through latches 1-3.Data to be written to the RAM is given through latches 4-5.The latches 6 and 7 are used to read the data from the RAM.

The component:

A.74LS374 OCTAL D-TYPE LATCHES: The SN74LS373 consists of eight latches with 3-state outputs for bus organized system applications.The data changes Asynchronously when Latch Enable (LE) is HIGH. When LE is LOW, the data is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state. The SN74LS374 is a high-speed, low-power Octal D-type Flip-Flop. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. Eight Latches in a Single Package. 3-State Outputs for Bus Interfacing. Edge-Triggered D-Type Inputs .Buffered Positive Edge-Triggered Clock.

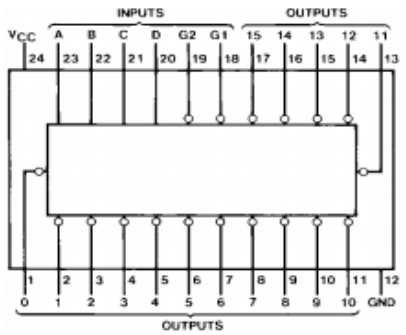




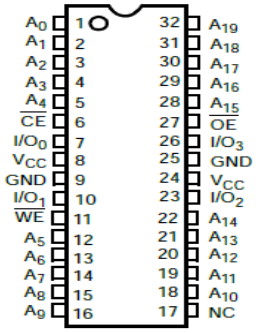
PIN NAMES	
$D_0 - D_7$	Data Inputs
LE	Latch Enable (Active HIGH) Input
CP	Clock (Active HIGH Going Edge) Input
OE	Output Enable (Active LOW) Input
$O_0 - O_7$	Outputs

***B.74LS154 4-LINE TO 16-LINE DECODER/DEMULTIPLEXER*:** Each of these 4-line-to-16-line decoders is used to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs G1 and G2 are LOW. The demultiplexing function is done by 4 input lines to address the output line, by sending data from one of the strobe inputs with the other input LOW. These demultiplexers are ideally suited for implementing high-performance memory decoders.

Connection Diagram



c.CY7C1046B – 1M X 4 STATIC RAM: The CY7C1046B is a high-performance CMOS static RAM organized as 1,048,576 words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE), an active LOW Output Enable (OE), and three-state drivers. Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the four I/O pins (I/O0 through I/O3) is then written into the location specified on the address pins (A0 through A19). Reading from the device is done by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pi*ns.*

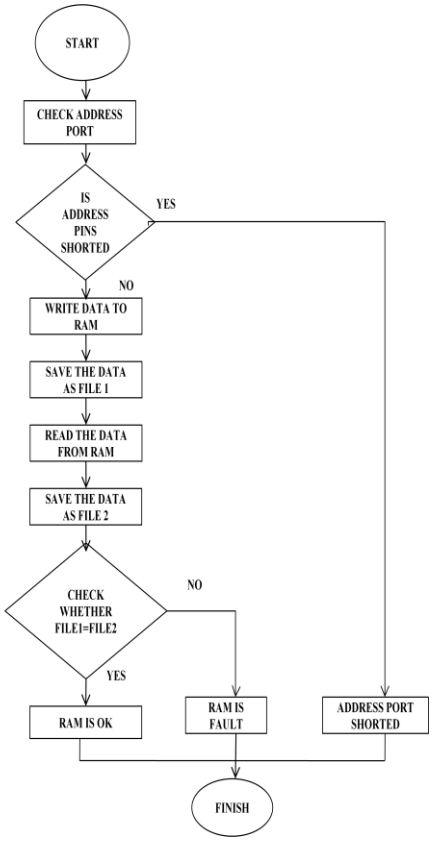


IV. OPERATION:

The memory section of the ACAJA5 which we are testing consists of 5 RAMs and 2 EPROMS.The RAM IC-CY7C104B has 1M storage location each of which can store 4bits of data hence we require 20 address bits to access each location. The NIC is designed to interface the ACAJA5 card with the parallel port of the PC.The control signals are generated by the program in VB in the EPP mode.

Latches 1, 2 and 3 are responsible for generating 20 bit address to RAM. Through EPP the LSB of address is given .In order to select the first 8 bits, we are outing the control signal 0001 via EPP. Similarly the next 12 bit of address lines are outed through latches 2-3.Now that we have generated the address, we can write the data given to the address .Giving the control signal 0100 via EPP LSB of the data enters latch4.Similarly the MSB of data enters latch5 by giving a control signal 0101.The Data will be written to the given address when the control signal 0110 to the RAM. Now that we have generated the address, we can read the data from the address. To read the signal to RAM/EPROM, the control signal 0111 is given via EPP.When another control signal 1000 is given latches 6 and 7 are clocked and data enters these latches. Output enable for latch 6, read value from EPP by giving control signal 1001, similarly output enable for latch7 read value from EPP by giving the control signal 1010.The data which was written previously in the memory was saved in a temporary location .The data which is read from the same location is compared with the saved data, for each of the memory locations. Message boxes showing memory status appear for each of the locations. We are simultaneously checking the 5 RAMs. The process of testing the entire RAM locations is completed within a few minutes.

FLOWCHART



V. CONCLUSION

The automated ACAJA5 Card Tester (ACT) is successfully completed and now we are able to test the memory section of the card consisting of 5 RAMs and 2 EPROMs within a very short time. The ACT enables any person, who just has basic ideas about using a computer, to perform functionality test of the complex ACAJA5 card with the very few mouse clicks. The conclusion here is that by using this project we enable to detect the faults, if any in the memory section of the ACAJA5 card of the OCB 283 exchange testing of the card manually using CRO and referring to the data sheet is a cumbersome task. Employing a PC for this purpose make a more efficient system. The interface card which we designed enables as to communicate between PC and ACAJA5 card. The software helps us to detect the fault in the card thus this is one of the most saving and efficient fault detecting mechanism

REFERENCES

[1] Kenneth G.Goad, Joseph G.Tront "Using Iterative Test Generation in a PC Based Guided Probe Testing System "- Virginia Polytechnic Institute and state university. *(references)*
[2] David M.Judge -"Trends in Automatic Testing Of Electronics Devices"-Giordano Associates Inc. 2006 Old Greenbrier Rd, Chesapeake.
[3] Venkata videhi Balusupati, Pavani Velaga, A.Rama Krishna- "Architecture of OCB-283 "– IJITEE, Volume-1, Issue-6, November 2012.K. Elissa, "Title of paper if known," unpublished.
[4] Visual Basic 6.0 – The complete reference Tata McGraw – Hill Edition
[5] Moore, Tim, and Garner, Stephen, "Auto-Probing on the L200 Functional Tester, '**I** 1985 International Test Conference.
[6] J. M. Corner, D i g i t an l Test Engineering. New York: John Wiley & Sons, 1987, ch. 11, pp. 286
[7] J. Turino, Design t o Test. New York: Van No strand Reinhold, 1990, ch. 6