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Depreciated built-in-self -test and built-in-self-repair scheme to amend all manufacturing faults

S.Saranya[1],(M.E AE), N.Narmatha[2], M.E.,
[1]Student/Dept of ECE, Anna University Chennai, [2]Assistant Professor/Dept of ECE, Anna University Chennai
Jayam College of Engineering and Technology, Dharmapuri DT, India

ABSTRACT
Reduction of static power and testing of the power switches has become the important nowadays in all VLSI manufacturing process. The proposed technique here is the Signature Analysis method to efficiently test the Power-switches. This concept gives us the technique to repair the Catastrophic and parametric faults including all manufacturing faults and also ability to tolerate the process variation. To perform the above signature analysis technique, a robust Built-In-Self-Test and Built-In-Self-Repair is used which is an very efficient and low cost testing method. Thus now the proposed technique has been modified with architectural change that still effectively detect the faults with less process variation and power dissipation and the comparative analysis of the voltage variations of the power gating structure is studied.

KEY WORDS -- *Built-in self-repair, Built-in self-test, , power switch test, process variation, tanner w-edit, modelism…*

I. INTRODUCTION

The reduction in transistor threshold voltages in deep sub micrometer technologies has led to unacceptably high static power consumption The method proposed in extends this approach to multiple intermediate power off modes: during the short periods of inactivity, the circuit is put into an appropriate power-off mode which is determined by both the wake-up time and the length of the idle period. Even though the architecture proposed in is effective for reducing leakage power during short periods of in activity, it cannot be extended to support more than two intermediate power-off modes, it is very sensitive to process variations and it is not-easily testable.

An efficient and robust architecture was proposed where it suitable for logic cores with specific requirements of static power dissipation and wake-up time; Power switches offer significant benefits in reducing static power

However, their adoption in practice depends on the availability of test and diagnosis methods.In this paper, a signature analysis method for the testing and diagnosis of the multimode power switches proposed where testing and diagnosing catastrophic and parametric faults affecting this architecture.

It also exploit inherent properties of the power-switch design, to develop a scheme to repair catastrophic and parametric faults, and to tolerate process variations at negligible cost. Finally, we propose a built-in self-test (BIST) / built-in self-repair (BISR) technique for testing and repairing multimode power switches. The BISR scheme provides a low-cost mechanism to repair faulty power switches

Power switches offer significant benefits in reducing static power. However, their adoption in practice depends on the availability of test and diagnosis methods. In prior work, test methods have been presented only for power switches that the multimode power-switch architecture proposed here for four per-off modes are Active, Sleep, Dream and Snore modes respectively.

II. PREVIOUS METHOD

The main objective of the project is to know the effect of catastrophic and parametric faults in-terms of voltage and wake up time. This project provides the capability to locate defects in these power mode switches and to identify the faults effectively. It also offers a very high tolerance to manufacturing defects.

The existing system uses a technique known as "SIGNATURE ANALYSIS TECHNIQUE" to test the power-switch. This technique provides tolerance to process variations and effectively diagnose the catastrophic and parametric faults using Built-In-Self-Test and Built-In-Self –Repair. Sudden and total failure from which recovery is impossible is known as catastrophic faults.

Any change in component value that causes the changes in output value results in fault known as parametric faults. But it has the several disadvantages like Static power dissipation is little higher. N-MOS are often susceptible to process variations comparatively Mis detections may occur often due to the sensitivity

III. III.PROPOSED METHOD

In this work, the effect of faults on ground voltage is computed using tanner software with less process variations compared to the previous method. This is done by means of changing the architectural components. From the change of the component their voltage variations are comparatively studied and analysis can be made which one can be used for the testing of power switches with less process variation .and detection and rectification faults can be detected more effectively.

Here several advantages could be achieved say Less power consumption**,** efficient tolerance for process variation, effective detection of faults. All these voltage variations and detection and repair of faults are achieved at very low cost.

IV. SIGNATURE BASED ANALYSIS

A. BIST STRUCTURE

The primary role of the BIST unit is to facilitate and automate the manufacturing test of the power switches. Without the BIST unit, special test equipment is required to read the analog voltage level at the virtual ground node, and a sophisticated communication protocol is needed between the Automatic Test Equipment (ATE) and the chip is needed to evaluate test responses in the presence of process variations. The block diagram of the BIST unit is shown in Fig. 1 (we assume that multimode power switch *Mj* is being tested). It receives various external signals that configure the operation of this structure .Signal *TEST_Go* initiates the test process, signal *Mode_ID* sets the power-off mode and signal *Sel_VCO* selects among the two *VCO* units available. The BIST unit generates signal *Test_end* to indicate when the test ends as well as the signal *Pass/Fail* to indicate whether the switch is good or not

The BIST circuitry consists of five main modules: the *VCO* unit that consists of *VCO-N* and *VCO-P* ring oscillators, the *VCO* counter, the auxiliary *Cycle* counter, the *FSM* (finite state machine) and a RO The *VCO* and the *VCO* counter operate as described in Section IV. The *Cycle* counter is used as an auxiliary counter to control the test periods that *VCO* counter counts up or down. The *FSM* is used to synchronize the operation of all units during BIST.

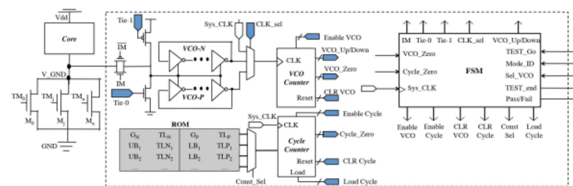


Fig 1: Bist umit.

The state transition diagram of the *FSM* for the casethat *VCO-N* is used for testing the power switches is illustrated in Fig. 2. There are two types of states: configuration states (*S*1, *S*3, *S*5, *S*7) and counting states (*S*2, *S*4, *S*6, *S*8).Configuration state *S*1 is used to setup the *VCO-N* for calculating the reference signature later at state *S*2.

Then at state*S*3 cycle counter is configured to subtract the golden reference signature from the *VCO* counter, and the subtraction is done at state *S*4. All these values are taken into account which is more effectively analysed. At state *S*5 the *VCO-N* is configured to add the upper bound *UBj* to the current contents of the *Cycle* counter, and generate thus the adjusted upper bound *UB adjj* .To this end the *Cycle* counter is loaded with the value of *UBj* and it counts down at state *S*6 until it reaches the value 0.At state *S*7 the *Cycle* counter is loaded with the time, as a number of system clock cycles *TLN* and *TLP* that is needed for the *VCO* counter to sample the *VCO-N* output. The *VCO-N* input is connected to *V_GND* and it begins triggering the *VCO* counter at state *S*8to subtract the upper signature bound from the *VCO* counter.

At this state the value of the signal *VCO_Zero* is monitored by the *FSM* and upon assertion of this signal the *FSM* reports failure (the power switch is defective).The state diagram for the *VCO-P* is similar to the state diagram of the *VCO-N.*

Note that for some power switches either the *VCO-N* or the *VCO-P* is used, while for other power switches both *VCO-N* and *VCO-P* are used. In the last case ,the power switch is considered defect-free if both *VCO-N,VCO-P* report successfully.

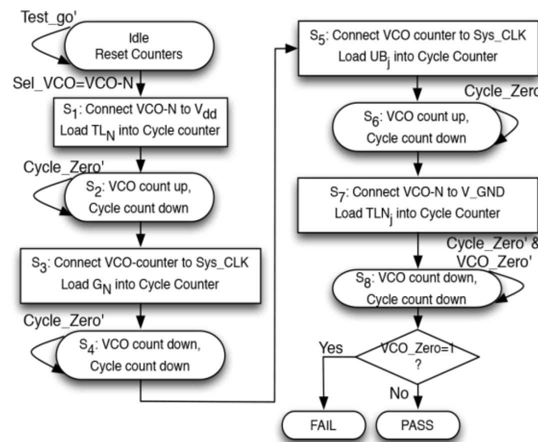


Fig 2: State diagram for BIST unit

B. BISR STRUCTURE

The repair mechanism inserts redundancy to replace any faulty power switch with spare fault-free switches .However, the selection of the non defective transistors can only be done post manufacture using programmable structures such as laser cut fuses or electrically programmable fuses (e-fuses) commonly used for memory built-in

Laser-cut fuses are characterized by high silicon area requirements(200μm2 per fuse is reported and they are not scalable with process evolution (they do not scale below the wavelength of the laser beam). In addition, they require a separate and time-consuming manufacturing flow, and this repair solution is not applicable after chip packaging.

On the other hand, e-fuses require a higher-than-nominal voltage for their programming, which must be either provided through an additional pad or generated by an embedded voltage generator (charge pump); both these solutions lead to substantial increase in chip cost whenever they are included in the design only for the purpose of repairing the power switches.

To alleviate the high cost associated with such approaches. I present a low-cost embedded solution. An additional module, the BISR unit, is embedded to coordinate the BIST session and to select one power switch for each power-off mode after the test is completed.

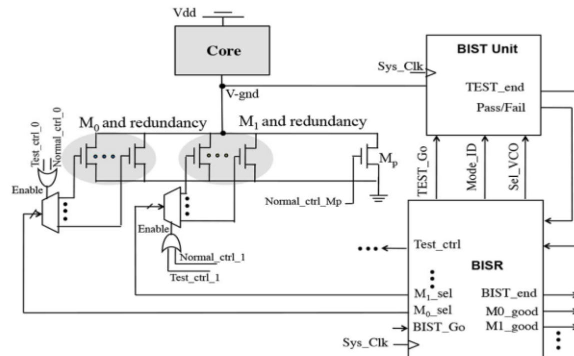


Fig 3: Complete BIST with Built-in-self- repair.

When the *BIST_Go* signal is asserted, the BISR unit selects the first power-off mode and it sets signal *Mode_ID* accordingly. Depending on the power-off mode it selects either the *VCO-N* or the *VCO-P* oscillator using signal *Sel_VCO*. In many cases it selects both of them one after the other and applies an independent test for each selected *VCO*.

Then, it selects one of the power switches for this mode it turns this switch on to put the core into the respective power-off mode, and it tests this power switch by asserting the *TEST_Go* signal of the BIST unit (note that the *BIST_Go* signal is used to turn-off the main power switch *MP* during the whole test period).

When the test finishes (the signal *TEST_end* is asserted) the status of the signal *Pass/Fail* is checked to verify whether the power switch passed the test or not.

If the power switch passed the test, it is selected as the power switch of the respective power-off mode and the rest of the power switches for the same power-off mode are not further exercised. To achieve maximum benefits in terms of static power dissipated, the power switches are tested one by one successively, starting from the switch with the smallest aspect ratio

. In that way, among the non defective switches that offer the required wake-up time, the smallest one is selected, which offers also the highest leakage power savings.

The flow diagram of the BISR operation is shown in the following figure.

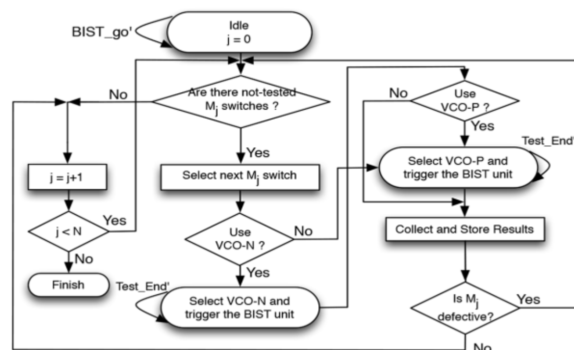


Fig.4: The state diagram of complete BIST and BISR scheme.

The proposed scheme receives a trigger signal (*BIST_Go*) from an external unit, and it begins to test the power switches starting from the group of *M*0 switches. It selects one *M*0 switch at a time until it finds a non defective one. Then, it proceeds to groups of *M*1,*M*2 switches (the next power-off modes). When all switches are tested, signal *BIST_end* is asserted to notify the external unit the end of the test operation

.The BIST and BISR units offer low-cost solutions to detect and repair power switches that fail either due to manufacturing defects or due to process variations. The use of spare power switches, combined with the use of multiple aspect ratios shifted above and below the nominal value, offer the means to counterbalance the effects of process variations and increase the process yield.

V. EXPERIMENTAL RESULTS

VA. VOLTAGE VARIATIONS USING TANNER SOFTWARE

The following voltage variation for the four types of power switch mode can be discussed here very clearly. The voltage variations of these modes is first drawn in the d calculus software for their schematic representation. Then this schematic can be converted in terms of the voltage variations of representing them in terms of 0's and 1's using the advanced software tanner s-edit.

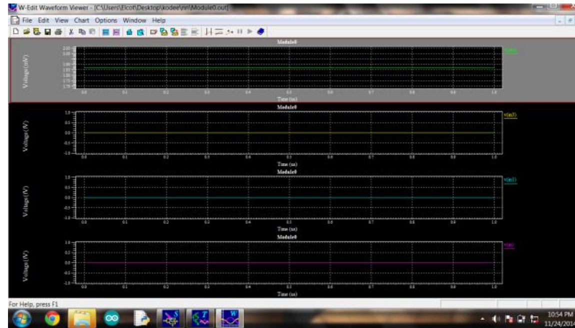


Fig 5.1 voltage variation of Snore mode

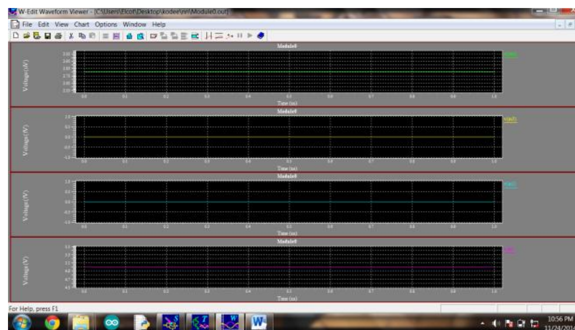


Fig 5.2 voltage variation of Dream mode

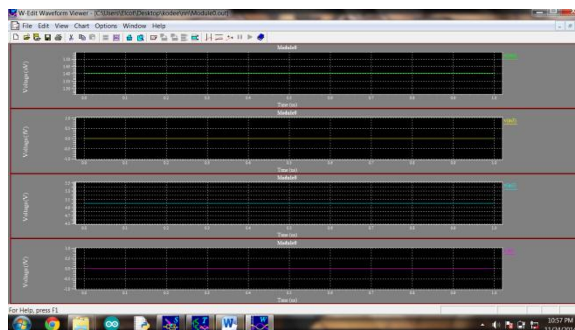


Fig 5.3 voltage variation of sleep mode

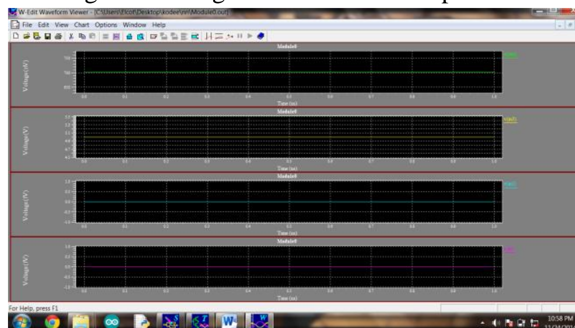


Fig 5.4 voltage variation of Nap mode

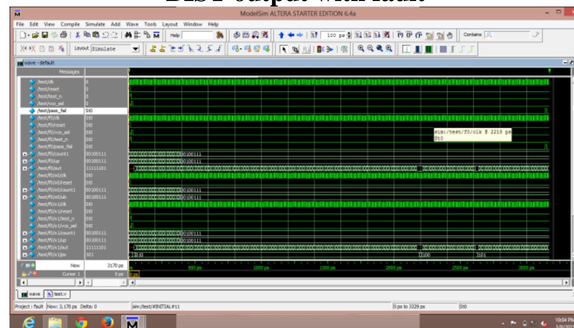
VB. THE TABLE WHICH SHOWS GROUND BOUNCING NATURE OF EACH MODE OF POWERSWITCH:

MODE	PRE-COMPUTED V-GND VALUES(mV)	COMPUTED V-GND USING NMOS VALUES	COMPUTED V-GND VALUES USING PSEUDO NMOS
snore	924	1.87 mV	3.52V
dream	496	2.8uV	910 mV
sleep	200	1.40uV	940mV
nap	99	700 nV	900 mV

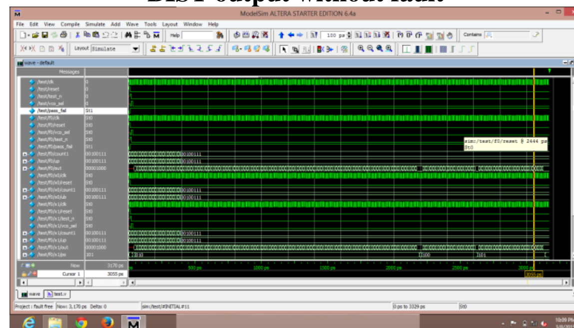
The first column reports the various power-off mode and the second reports the voltage at the *V_GND* node of pre computed values at each of this mode. The third column presents the positive ground bounce peak during the activation of the core from any power-off mode. The last two columns present the importance voltage variations by using the advanced software tool say tanner w-edit of nmos and pseudo nmos respectively. From this such minute variations it is very useful for designing the most accurate power switch design for the testing purposes.

It also provides us less power dissipation with tolerance to process variations.**The simulated results** using modelsim software of bist unit with faulty switch and without fault are shown below. The switch that is faulty is replaced by the redundancy switch is also determined by the simulation using modelsim software.

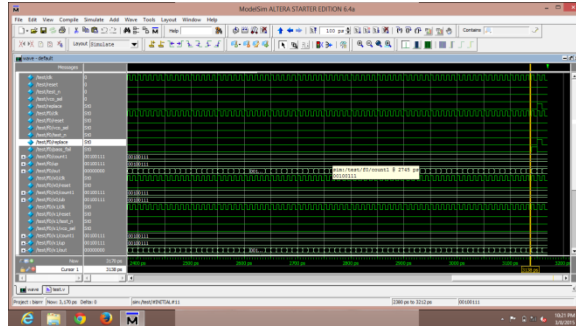
BIST output with fault



BIST output without fault



BISR Output



FAULT ANALYSIS

CATEGORY	REF VALUE	CYCLE COUNT	VOLTAGE VARIATIONS
NMOS	Rn=222	50	V,mV,Uv,nV
PSEUDO NMOS	Rn=300(assume)	68	V,mV

VI. VI.CONCLUSION

Thus, the proposed system modifies the conventional method of using signature based analysis to test the power switches more effectively by means of depreciated BIST and BISR scheme to effectively detect the manufacturing fault and replace such a faulty switch with sparse switches which is effectively done by means of the BISR scheme. Finally, the effect of faults on ground voltage(v) an will be reduced about 5 % of the previous method. This is done by means of changing the architectural components. From the change of the component their detection and rectification faults can be detected with less process variations.And finally the comparative analysis of the voltage variations with the architectural change is studied more effectively with less power consumption and detection of faults.

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