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A New Rv Multilevel Inverter For Induction Motor Drive Applications

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----------ABSTRACT----------

In recent years, multilevel inverters have gained much attention in the application areas of medium voltage and high power owing to their various advantages such as lower common mode voltage, lower voltage stress on power switches, lower dv/dt ratio to supply lower harmonic contents in output voltage and current. Comparing two-level inverter topologies at the same power ratings, MLIs also have the advantages that the harmonic components of line-to-line voltages fed to load are reduced owing to its switching frequencies. The most common MLI topologies classified into three types are diode clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI), and cascaded H-Bridge MLI (CHB-MLI). The hybrid and asymmetric hybrid inverter topologies have been developed according to the combination of existing MLI topologies or applying different DC bus levels respectively. This paper proposes a new Multilevel Inverter for Induction Motor Drive. The Inverter presented gives a seven level output voltage. This inverter uses very less number of switches when compared with the other type of multi inventers like diode clamped, flying capacitor, and cascaded inventers. This topology requires very less number of carrier signals and gate drivers, especially when used for higher levels. The above discussed inverter is fed to a induction motor drive and the performance of the motor is analyzed for nine level and eleven levels.

INDEX TERMS: ***MLI*** *(multilevel inverter), Reversing Voltage Multilevel topology, SPWM technology.*

I. INTRODUCTION

Multilevel power conversion was first introduced more than two decades ago. This concept explains the utilization higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with the conventional power conversion approach. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce voltage (*dv/dt*) stress on the load and the electromagnetic compatibility concerns [1]. Another important feature of multilevel converters is that the Semiconductors are connected in series, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. One clear disadvantage of multilevel power conversion is the higher number of semiconductor switches required. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors [2].

However, the most recently used inverter topologies, which are mainly addressed as applicable multilevel inverters, are cascade converter, neutral-point clamped (NPC) inverter, and flying capacitor inverter. There are also some combinations of the mentioned topologies as series combination of a two-level converter with a three-level NPC converter which is named cascade 3/2 multilevel inverter [3]. There is also a series combination of a three-level cascade converter with a five-level NPC converter which is named cascade 5/3 multilevel inverter [4].Some applications for these new converters include industrial drives [5], flexible ac transmission systems (FACTS) [6]–[7],and vehicle propulsion [8], [9]. One area where multilevel converters are particularly suitable is that of renewable photovoltaic energy that efficiency and power quality are of great Concerns for the researchers [10].Some new approaches have been recently suggested such as the topology utilizing low-switching-frequency high-power devices [11]. Although the topology has some modification to reduce output voltage distortion, the general disadvantage of this method is that it has significant low-order current harmonics. It is also unable to exactly manipulate the magnitude of output voltage due to an adopted pulse width modulation (PWM) method [12].In [13] and [14], the multilevel output is generated with a multi winding transformer.

However, the design and manufacturing of a multi winding transformer are difficult and costly for high- power applications. This is a disadvantage of the proposed inverter, particularly when it should output low or zero voltage to a load [15]. Another approach is selection based on a set target which can be either the minimum switches used or the minimum used dc voltage. It also requires different voltage source values which are defined according to the target selection. However, this approach also needs basic units which are connected in series, and the basic units still require more switches than the proposed topology. Another disadvantage of the topology is that the power switches and diodes also need to have a different rating which is a major drawback of the topology.

The proposed topology is a symmetrical topology since all the values of all voltage sources are equal. However, there are asymmetrical topologies, which require different voltage sources. This criterion needs to arrange dc power supplies according to a specific relation between the supplies. Difference in ratings of the switches in the topology is also a major drawback of the topology. This problem also happens in similar topologies, while some of the high-frequency switches should approximately withstand the maximum overall voltage which makes its application limited for high-voltage Products. Some of the proposed topologies suffer from complexities of capacitor balancing. This paper presents an overview of a new multilevel inverter topology named reversing voltage (RV). This topology requires less number of components compared to conventional topologies. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter. This paper describes the general multilevel inverter schematic. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels. The simulation and experimental results of the proposed topology are also
presented.

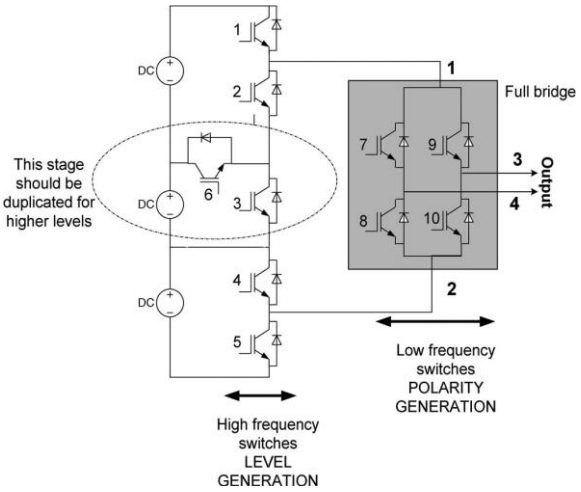

Fig. 1. Schematic of a seven-level inverter in single phase.

II. NEW MULTILEVEL TOPOLOGY

2.1. General Description

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named *level generation* part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called *polarity generation* part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and Low frequency) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities.

The RV topology in seven levels shown in Fig.1. As can be seen, it requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage in Fig. 1 generates the required output levels (without polarity) and the right circuit (full-bridge converter) decides about the polarity of the output voltage. This part, which is named polarity generation, transfers the required output level to the output with the same direction or opposite direction according to the required output polarity. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity.

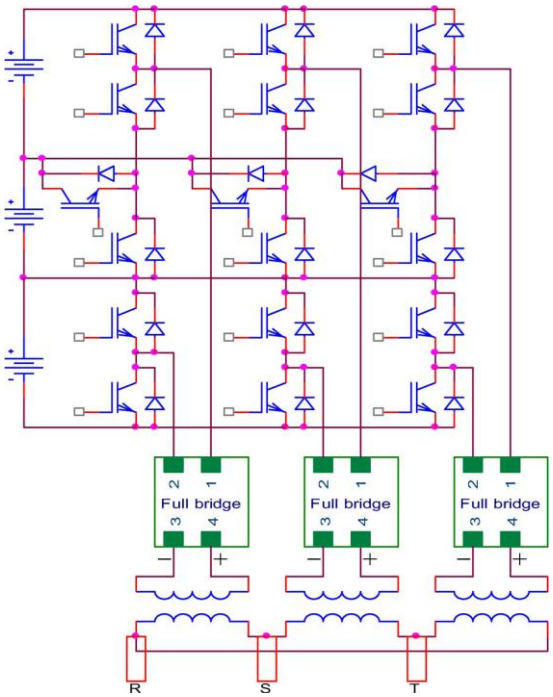

Fig. 2. Three-phase RV multilevel topology

This topology easily extends to higher voltage levels by duplicating the middle stage as shown in Fig. 1. Therefore, this topology is modular and can be easily increased to higher voltage levels by adding the middle stage in Fig. 1.It can also be applied for three-phase applications with the same principle. This topology uses isolated dc supplies. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. In Fig. 2, the complete three-phase inverter for seven levels is shown with a three-phase delta connected system. According to Fig. 2, the multilevel positive voltage is fed to the full-bridge converter to generate its polarity. Then, each full bridge converter will drive the primary of a transformer. The secondary of the transformer is delta (Δ) connected and can be connected to a three-phase system. This topology requires fewer components in comparison to conventional inverters. Another advantage of the topology is that it just requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists Of six carriers, but in this topology, three carriers are sufficient. The reason is that, according to Fig. 1, the multilevel converter works only in positive polarity and does not generate negative polarities. Therefore, it implements the multilevel inverter with a reduced number of carriers, which is a great achievement for inverter control. It is also comparable to single-carrier modulation

TABLE I.
SWITCHING SEQUENCES FOR EACH LEVEL

Level / Mode	0	1	2	3
1	2,3,4	2,3,5	1,4	1,5
2		2,4,6	2,6,5	

6while this topology requires the same number of signals for PWM. However, this topology needs one modulation signal which is easier to generate as opposed to the single-carrier modulation method which needs several modulation signal.

2.2. Switching Sequences : Switching sequences in this converter are easier than it's Counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency then, this level is translated to negative or positive according to output voltage requirements. This topology is redundant and flexible in the switching sequence. Different switching modes in generating the required levels for a seven-level RV inverter are shown in Table I. In Table I, the numbers show the switch according to Fig. 1 which should be turned on to generate the required voltage level. According to the table, there are six possible switching Patterns to control the inverter. It shows the great redundancy of the topology. However, as the dc sources are externally adjustable sources (dc power supplies), there is no need for voltage balancing for this work.This will also help to decrease switching power dissipation .According to the aforementioned suggestions, the sequences of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively. These sequences are shown in Fig. 3. As can be observed from Fig. 3, the output voltage levels are generated in this part by appropriate switching sequences. The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold .In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required as shown in Fig. 4. Carriers in this method do not have any coincidence, and they have definite offset from each other. They are also in phase with each other.

The modulator and three carriers for SPWM are shown in Fig.4

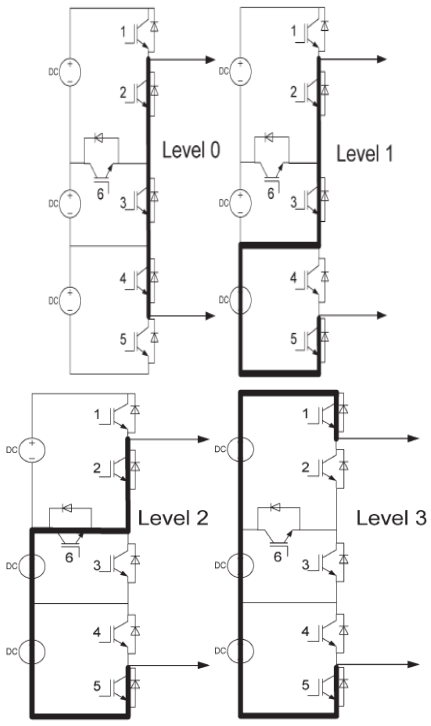

Fig. 3. Switching sequences for different level generation.

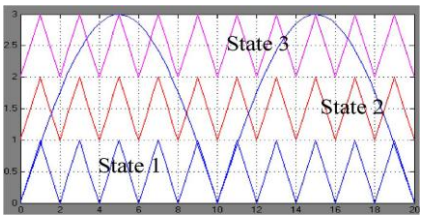

Fig. 4. SPWM carrier and modulator for RV topology

TABLE II
SWITCHING CASES IN EACH STATE ACCORDING TO RELATED COMPARATOR OUTPUT

States	One		two		Three	
Compare	+	-	+	-	+	-
Mode	2-3-5	2-3-4	2-5-6	2-3-5	1-5	2-5-6

According to Fig. 4, three states are considered. The first State is when the modulator signal is within the lowest carrier. The second state is when it is within the middle carrier. Finally, the third one is when it is within the highest carrier. In each state, certain switching patterns are adopted to cover the voltage requirements. According to this definition, the switching states and switching modes are described in Table II. It shows the relation between the right comparator output according to the current state and required states for switching to meet the voltage requirements. The right comparator here refers to the comparator output of the current state. As component of the inverter. Illustrated in Table II, the transition between modes in each state requires minimum commutation of switches to improve the efficiency of the inverter during switching states. The number of switches in the path of conducting current also plays an important role in the efficiency of overall converter. For example, a seven-level cascade topology has 12 switches, and half of them, i.e., six switches, conduct the inverter current in each instance. However, the number of switches which conduct current in the proposed topology ranges from four switches (for generating level 3) to five switches conducting for other levels, while two of the switches are from the low-frequency (polarity generation) component of the inverter.

Therefore, the number of switches in the proposed topology that conduct the circuit current is lower than that of the cascade inverter, and hence, it has a better efficiency. The same calculation is true in a topology mentioned. The least number of switches in the current path for a seven-level inverter according to is five (for generating level 3), which requires one switch more in the current path compared to the proposed topology which requires only four conducting switches.These switching sequences can be implemented by logic gates or DSP. Low-frequency output stage is an H-bridge inverter and works in two modes: forward and reverse modes. In the forward mode, switches 8 and 9 as in Fig. 1 conduct, and the output voltage polarity is positive. However, switches 7 and 10 conduct in reverse mode, which will lead to negative voltage polarity in the output. Thus, the low-frequency polarity generation stage only determines the output polarity and is synchronous with the line frequency. The resulting PWM waveforms for driving the high frequency switches in the level generation part are illustrated for one complete cycle in Fig. 5. According to Fig. 5, high frequency switches can be adopted in this stage based on the required frequency and voltage level.

2.3. Number of Components : As mentioned earlier, one of the promising advantages of the topology is that it requires less high-switching-frequency components. According to the MIL-HDBK-217F standard, the reliability of a system is indirectly proportional to the number of its components.Therefore, as the number of high-frequency switches is increased, the reliability of the converter is decreased.

TABLE.III.
Comparison of proposed topology with Other topologies.

Inverter type	NPC	Flying capacitor	Cascade	RV
Main switches	6(N-1)	6(N-1)	6(N-1)	3((N-1)+4)
main diodes	6(N-1)	6(N-1)	6(N-1)	3((N-1)+4)
Clamping diodes	3(N-1)(N-2)	0	0	0
DC bus capacitors/ Isolated supplies	(N-1)	(N-1)	3(N-1)/2	(N-1)/2
Flying capacitors	0	$\frac{3}{2}$(N-1)(N-2)	0	0
Total numbers	(N-1)(3N+7)	$\frac{1}{2}$(N-1)(3N+20)	$\frac{27}{2}$(N-1)	(13N+35)/2

III. MATLAB/SIMULINK MODELLING AND SIMULATION RESULTS.

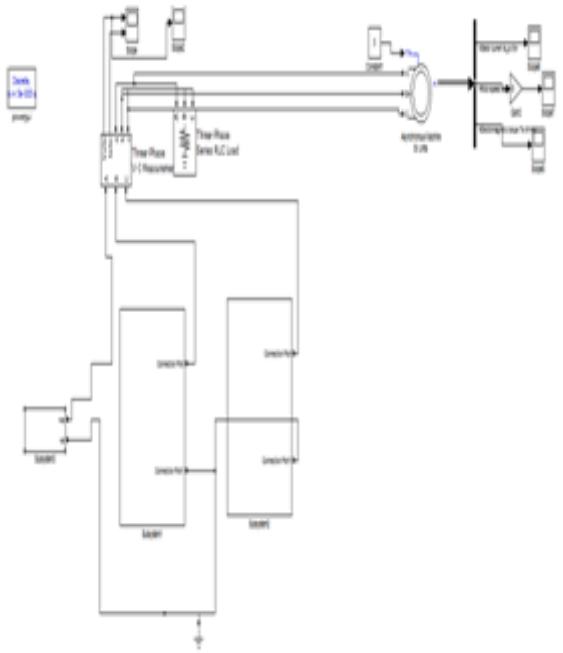

Fig.5. the above figure shows the simulation of induction motor drive

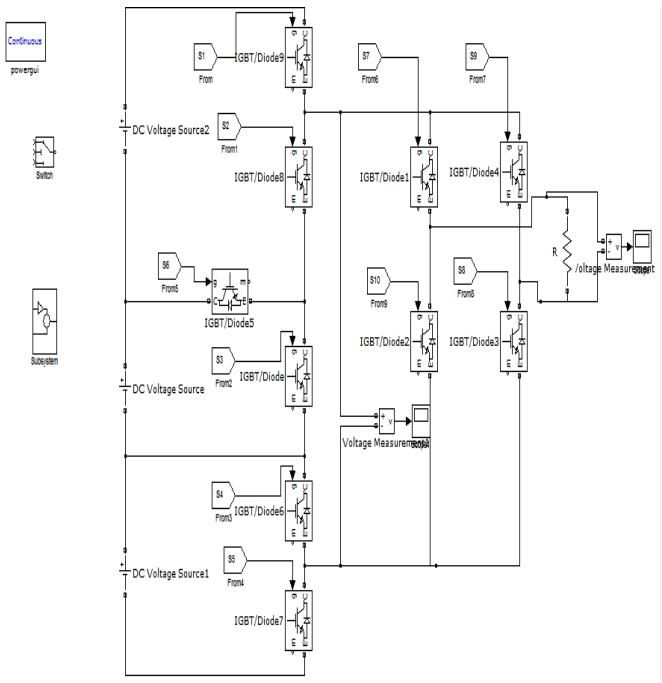

Fig.6. The above figure shows the Simulation Circuit diagram Single phase Seven Level Inverter

In the above fig shows the simulation of seven level inverter consisting Of ten switches and three isolated sources at an instant minimum two Switches are conducted from level generation part and two from Polarity generation part, and gate drives are required for every IGBT these drives are received from the control circuit.

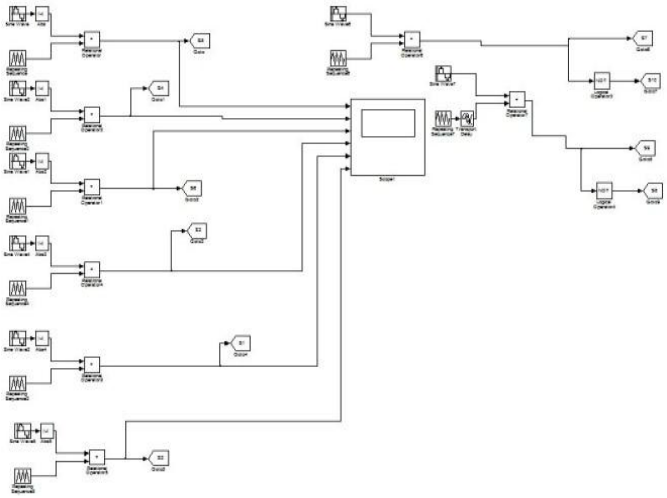

Fig.7 The above figure shows the Simulation Control Circuit of Single Phase Seven Level Inverter

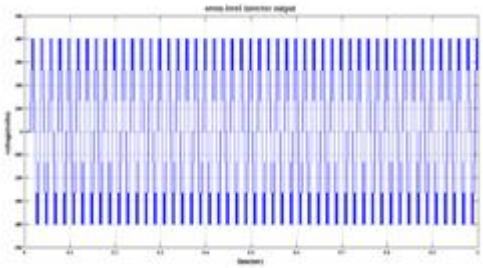

Fig. 8 Seven level inverter output

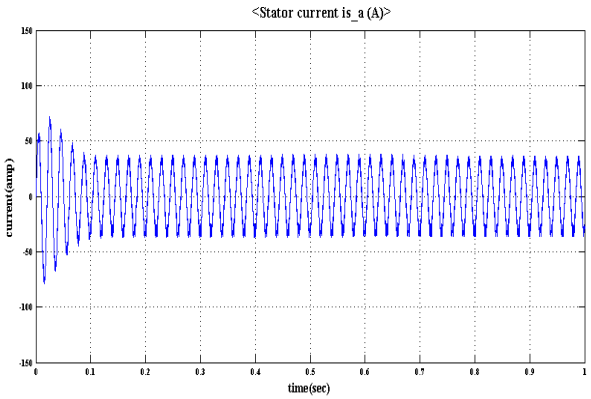

Fig.9.stator current of induction motor

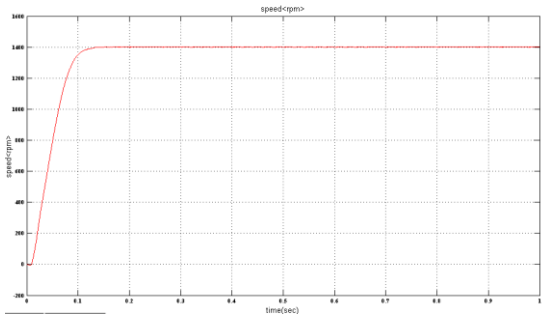

Fig.10.speed wave form of induction motor

Fig 11.torque wave form of induction motor

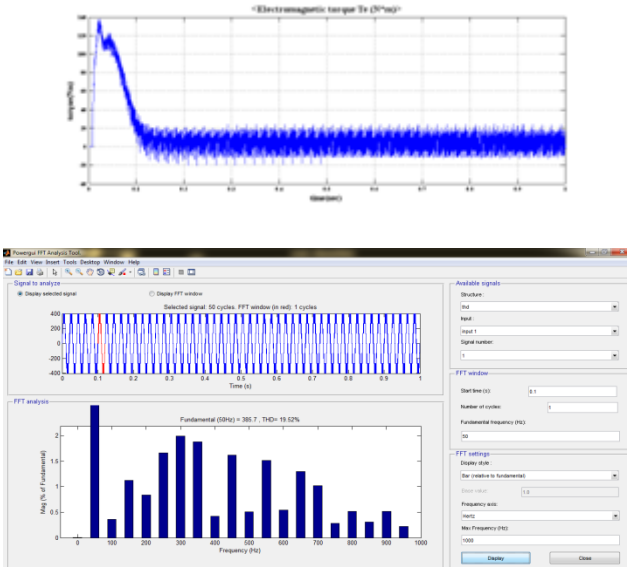

Fig.12.FFT analysis of stator current with seven level inverter

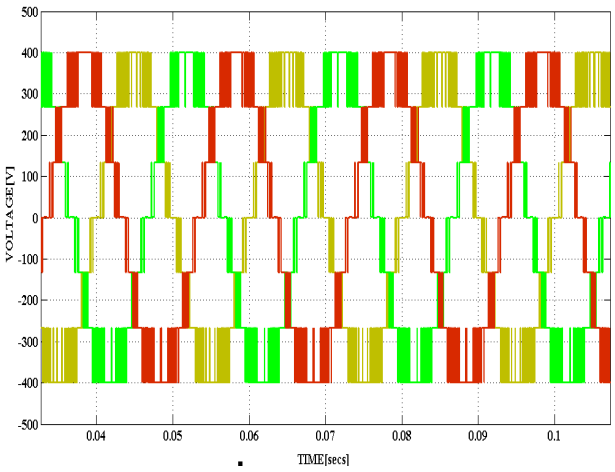

Fig 13.three phase output of induction motor

IV. CONCLUSION

In this paper, a new inverter topology for induction motor drive has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the mentioned topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. The experimental results of the developed prototype for a seven-level inverter and nine level inverter of the induction motor are demonstrated in this paper. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of carriers for PWM. It can also extent to eleven levels on so on.

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