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A Novel Approach of Active NPC (ANPC) Multi Level Inverters for Fault-Tolerant Operation

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----------ABSTRACT----------
Compared with neutral-point-clamped (NPC) inverters, active NPC (ANPC) inverters enable a significantly improved output power and performance for high-power electrical drives. This paper analyzes the operation of three-level (3L) ANPC inverters under device failure conditions, and proposes the fault-tolerant strategies to enable continuous operating of the inverters and drive systems under single device open and short failure conditions. Therefore, the reliability and robustness of the electrical drives are greatly improved. Moreover, the proposed solution adds no additional components to standard 3L-ANPC inverters; thus, the cost for robust operation of drives is lower. Simulation results are provided for verification. The results show that 3L-ANPC inverters have higher reliability than 3L-NPC inverters when a de-rating is allowed for the drive system under fault-tolerant operation.

KEYWORDS: Active NPC (ANPC), multilevel inverters, fault tolerant, reliability.

I. INTRODUCTION

Multi-level Inverters have found successful applications in medium voltage high-power electrical drives, Such as mining, pumps, fans and tractions. Since multilevel inverters have a large number of power devices, any device failure may cause the abnormal operation of the electrical drives, and require shutdown of the inverter and the whole sys- tem to avoid further serious damage. However, in some critical industrial processes with high standstill cost and safety-aspect concern, a high reliability and survivability of the drive system is very important. Therefore, fault-tolerant operation of multilevel inverters has drawn lots of interest in recent years, and several researchers have addressed the fault-tolerant issues for the popular multilevel topologies, such as neutral-point-clamped (NPC) inverters [1]–[7], flying capacitor inverters, cascaded H-bridge inverters, and generalized inverters. In most fault-tolerant solutions, additional components (such as power devices, fuses, or even phase legs) are required to be added to standard multilevel inverters for fault-tolerant operation. This will increase the cost and may even reduce the reliability of the inverters and drive systems due to employing more components. Moreover, both device open and short fail- ure may occur in the inverters, depending on the characteristics and failure mechanism of power devices; thus, a comprehensive fault-tolerant scheme should consider both failure conditions. Recently, three-level (3L) active NPC (ANPC) inverters were proposed to overcome the unequal power loss distribution among the semiconductor devices in NPC inverters, thus, enabling a substantially increased output power and an im- proved performance for high-power electrical drives [8], [9]. This paper analyzes the operation of 3L-ANPC inverters under device failure conditions and proposes the fault-tolerant strategies to enable continuous operation of the inverters and drive systems for single device open and short failure. Therefore, the reliability and robustness of the inverters and electrical drives are greatly improved. More- over, since the proposed solution adds no additional components to standard 3L-ANPC inverters, the cost for robust operation of drives is lower. Simulation results are provided for verification. The results show that 3L-ANPC inverters have higher reliability than 3L-NPC inverters when a de-rating is allowed for the drive system under fault-tolerant operation.

II. FAULT-TOLERANT DESIGN OF 3L-ANPC INVERTERS

A. Operation Analysis of 3L-ANPC Inverters under Device Failure Conditions

Fig. 1 shows the circuit of a 3L-ANPC inverter. The relation of switching states, switching sequence,

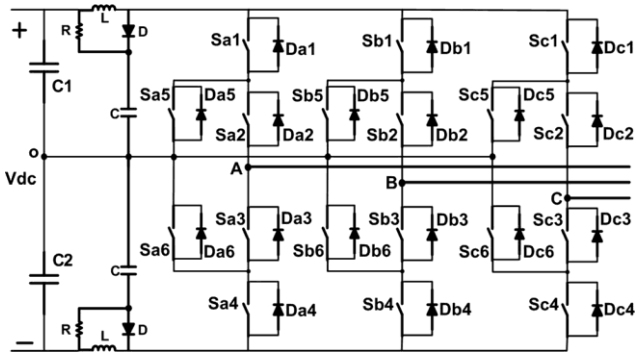

Fig. 1. Circuit of a 3L-ANPC inverter

and output voltage for phase A of the inverter is given in Table I. In normal operation (no device failure occurs), one of the four zero switching states (0U1/0U2/0L1/0L2) is selected to balance the power loss distribution among the devices in the inverter [25]. Under device failure condition, due to the symmetrical structure of 3L-ANPC topology, the failure of S_{a1}/D_{a1} and S_{a4}/D_{a4} has similar effects on the inverter, and this is also valid for the other pairs: S_{a2}/D_{a2} and S_{a3}/D_{a3}, S_{a5}/D_{a5}, and S_{a6}/D_{a6}. Therefore, only one from each pair of the devices in phase A will be analyzed in the following fault analysis.

Table I
Switching states, Switching sequence, and output voltage of a 3L-ANPC Inverter

Switching states	Switching sequence						Output voltage
	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	
+	1	1	0	0	0	1	+Vdc/2
0U2	0	1	0	0	1	0	0
0U1	0	1	0	1	1	0	0
0L1	1	0	1	0	0	1	0
0L2	0	0	1	0	0	1	0
-	0	0	1	1	1	0	-Vdc/2

Fig. 2 shows the examples of the current flow path at different output voltage levels under the open failure of S_{a1}/D_{a1}, S_{a2}/D_{a2}, and S_{a5}/D_{a5}, respectively. The positive current direction is defined as flowing out of the phase. As seen, when S_{a1} open failure occurs at "+" state, if $I_a > 0$, as shown in Fig. 2(a), then the phase output is connected to neutral-point (NP) of dc- link instead of positive dc bus. In Fig. 2(c), S_{a2} open failure occurs at "0U2/0U1" state when $I_a > 0$, then the phase output is connected to negative dc bus rather than NP of dc-link. Fig. 2(d) shows that S_{a5} open failure occurs at "0U2/0U1" state when $I_a < 0$, then the phase output is connected to positive dc bus instead of NP of dc-link. Due to the incorrect output voltage, the output current will become unsymmetrical and the NP of dc-link will be unbalanced. When D_{a1} open fault occurs at "+" state and $I_a < 0$, as shown in Fig. 2(b), the condition is even worse since the phase current I_a becomes discontinuous due to the cutoff of conduction path, then the induced voltage on load inductor and loop inductor may cause overvoltage on the inverter and cause damage. For other device failure cases, the circuit can be analyzed in the similar way.

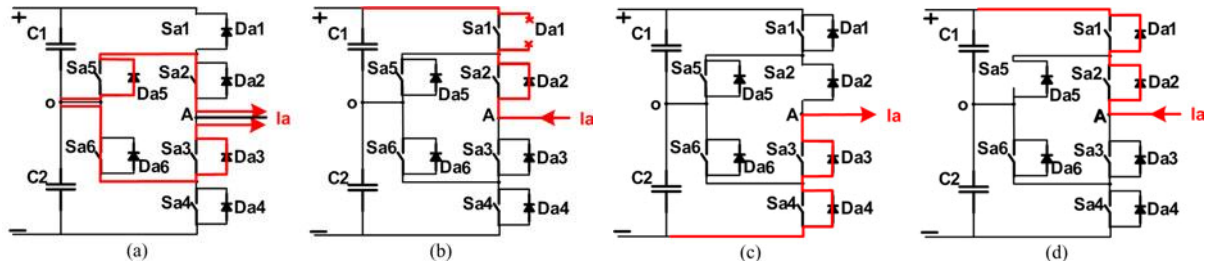

Fig. 2.Examples of current flow path under single device open failure in 3L- ANPC inverters: (a) $Sa1$ open-fail, + state, Ia >0. (b) $Da1$ open-fail, + state, Ia <0. (c) $Sa2$ open-fail, 0U2/0U1 state, Ia >0. (d) $Sa5$ open-fail, 0U2/0U1 state, Ia < 0.

Device short failure can cause even more serious problems compared to open failure. The reason is that under short-failure condition, the dc-link capacitors may be discharged through a short-current conduction path directly, and some devices may break down due to over current. Moreover, because the voltage of one dc-link capacitor will drop to zero quickly, other de- vices may have to withstand the full dc bus voltage and break down due to overvoltage. If we assume that the capacitors and devices can survive in this condition, the inverter output cur- rents will become unbalanced. Fig. 3 shows the current flow path under short failure of $S_{a\,1}/D_{a\,1}$, $S_{a\,2}/D_{a\,2}$, and $S_{a\,5}/D_{a\,5}$, respectively.

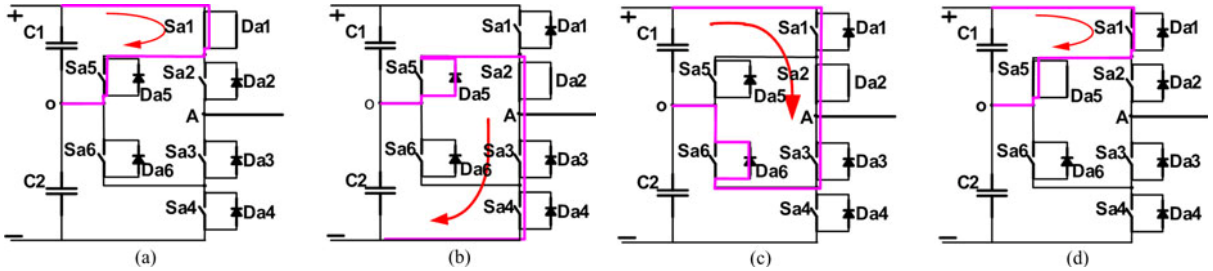

Fig. 3. Examples of current flow path under single device short failure in 3L- ANPC inverters. (a) $Sa1/Da1$ short-fail, 0U1/0U2/- state. (b) $Sa\,2/Da2$ short- fail, – state. (c) $Sa2/Da2$ short-fail, 0L1 state. (d) $Sa5/Da5$ short-fail, +/0L1 state.

When $S_{a\,1}/D_{a\,1}$ short failure occurs, if the switching state commutates to "0U1/0U2/−," as shown in Fig. 3(a), the upper capacitor C_1 will be shorted by $S_{a\,1}/D_{a\,1}$ and S_{a5}. Fig. 3(b) and (c) shows that if $S_{a\,2}/D_{a\,2}$ short failure occurs, "−" state forms a short-current path for lower capacitor C_2, while C_1. If $S_{a\,5}/D_{a\,5}$ short failure occurs at "+/0L1" state, as shown in Fig. 3(d). The condition is same as the Fig. 3(a).

Table II
Solution for single device open failure of a 3L-ANPC Inverter

Fault device	Switching states	Switching sequence						Output voltage
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	
Sa5 /Da5	+	1	1	0	0	0	1	+Vdc/2
	0L1	1	0	1	0	0	1	0
	0L2	0	0	1	0	0	1	
	-	0	0	1	1	0	0	-Vdc/2
Sa6 /Da6	+	1	1	0	0	0	0	+Vdc/2
	0U2	0	1	0	0	1	0	0
	0U1	0	1	0	1	1	0	
	-	0	0	1	1	1	0	-Vdc/2
Sa1 /Da1	0U2	0	1	0	0	1	0	0
	0L2	0	0	1	0	0	1	
Sa2 /Da2	0L2	0	0	1	0	0	1	0
Sa3 /Da3	0U2	0	1	0	0	1	0	0
Sa4 /Da4	0U2	0	1	0	0	1	0	0
	0L2	0	0	1	0	0	1	

B. Proposed Fault-Tolerant Strategies of 3L-ANPC Inverters : *1) Single Device Open Failure of 3L-ANPC Inverters:* Be- sides the power loss balancing function, the ANPC switches S_{a5} and S_{a6} can also provide a fault-tolerant ability for the inverter. The modified switching states and switching sequences for the fault-tolerant operation under single device open failure are given in Table II. After device open failure is detected, the 3L-ANPC inverter transits from normal operation into fault- tolerant operation. Knowing the position of the failed device, a new switching sequence is selected to generate certain switching state according to Table II.As seen, if S_{a5}/D_{a5} or S_{a6}/D_{a6} fails open, the 3L-ANPC inverter is derived into a similar configuration as the conventional 3L-NPC inverter. The faulty phase is still able to output three voltage levels, and the maximum modulation index and the out- put voltage waveform quality are the same as normal operation. Moreover, the device power loss balancing function can still be implemented to some extent during fault-tolerant operation. For example, if only S_{a5} fails, while D_{a5} is healthy, then besides the "0L1" and "0L2" switching states, the faulty phase can still generate "0U1" and "0U2" switching states when the phase current is positive, which can be used for power loss balancing. If any single device open failure occurs among S_{a1}/D_{a1} through S_{a4}/D_{a4}, the output terminal of the faulty phase needs to be connected to the NP of dc-link. The modulation signals also need to be modified in order to maintain the balanced three- phase line-to-line voltages.

In carrier-based SPWM modulation of 3L-ANPC inverters, the references of the phase voltages in normal operation are expressed by (1). In this paper, we assume the maximum modulation index is 1 for linear modulation under normal operation. It is worth to mention that if zero-sequence component injection is used for SPWM modulation, the maxi- mum modulation index can reach 1.15 under normal operation. However, since zero-sequence component injection is not the focus of this paper, we do not discuss this aspect in the following sections. When the faulty phase can only output "0" voltage level, instead of using the balanced phase voltages as the reference signals, we must modify the reference signals to ensure that the line-to-line voltages are balanced in 3L-ANPC inverters. Therefore, a new set of phase voltage references is provided in (2). As seen, to avoid over modulation, the maximum modulation index is limited to 0.577 during fault-tolerant operation, which is 1/3 of that in normal operation. Moreover, the freedom degree of zero-sequence component injection is also lost for the SPWM modulation.

$$\left.\begin{aligned} V_a &= m\sin(wt) \\ V_b &= m\sin(wt-2\pi/3) \\ V_c &= m\sin(wt+2\pi/3) \end{aligned}\right\} \quad (1)$$

$$\left.\begin{aligned} V_a &= 0 \\ V_b &= -\sqrt{3}*m\sin(wt+\pi/6) \\ V_c &= \sqrt{3}*m\sin(wt+2\pi/3+\pi/6) \end{aligned}\right\} \quad (2)$$

Where m is modulation index, V_a, V_b, and V_c are phase voltage references, and ω is fundamental frequency

2) Single Device Short Failure of 3L-ANPC Inverters: For device short failure, we need to avoid using the switching states and switching sequences that can construct short-current path for the dc-link capacitors. Two solutions are proposed here.

Table III

Solution I for single device short failure of a 3L-ANPC Inverter

Fault device	Switching states	Switching sequence						Output voltage
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	
Sa1 /Da1	+	0	1	0	0	0	1	+Vdc/2
	0	0	0	1	0	0	1	0
	-	0	0	1	1	0	0	-Vdc/2
Sa2 /Da2	0	0	0	0	0	1	0	0
Sa3 /Da3	0	0	0	0	0	0	1	0
Sa4 /Da4	+	1	1	0	0	0	0	+Vdc/2
	0	0	1	0	0	1	0	0
	-	0	0	1	0	1	0	-Vdc/2
Sa5 /Da5	0	0	1	0	0	0	0	0
Sa6 /Da6	0	0	0	1	0	0	0	0

In solution I, the modified switching states and switching sequences are given in Table III. In this scheme, when $S_{a\,1}/D_{a\,1}$ or $S_{a\,4}/D_{a\,4}$ has short failure, the faulty phase can still output three voltage levels by choosing proper switching sequence; thus, the output voltage and current of the inverter are almost the same as those in normal operation. For the other device short-failure cases, we can use the similar method as that for device open failure to connect the faulty phase to the NP of dc-link, and modify the reference signals as (2). Accordingly, the maximum modulation index will be reduced to 0.577. However, the draw- back of solution I is that certain devices have to withstand the full dc bus voltage under $S_{a\,1}/D_{a\,1}$ or $S_{a\,4}/D_{a\,4}$ short-failure condition. For example, when $S_{a\,1}/D_{a\,1}$ fails short, overvoltage will appear across $S_{a\,2}/D_{a\,2}$ at "−" state according to Table III. Similarly, when $S_{a\,4}/D_{a\,4}$ fails short, the voltage across $S_{a\,3}/D_{a\,3}$ will be full DC bus voltage at "+" state. For a standard 3L-ANPC inverter, the voltage rating of the employed power devices is lower than the dc bus voltage (theoretically, equal to half of the dc bus voltage). For example, a 3L-ANPC inverter with 5-kV dc bus voltage usually employs 4.5-kV power devices. Therefore, some devices may take the risk to break down due to overvoltage during fault-tolerant operation with solution I.

Table IV
Solution II for single device short failure of a 3L-ANPC Inverter

Fault device	Switching states	Switching sequence						Output voltage
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	
Sa1/Da1	0	0	0	1	0	0	1	0
Sa2/Da2	0	0	0	0	0	1	0	0
Sa3/Da3	0	0	0	0	0	0	1	0
Sa4/Da4	0	0	1	0	0	1	0	0
Sa5/Da5	0	0	1	0	0	0	0	0
Sa6/Da6	0	0	0	1	0	0	0	0

To overcome the drawback of the first solution, solution II is proposed, as shown in Table IV. In this scheme, no matter which device fails in short, the faulty phase is always connected to the NP of dc-link, and the reference signals are modified according to (2). By doing so, the maximum modulation index will be reduced to 0.577 and the output power rating of the 3L-ANPC inverter will be reduced. However, overvoltage will not appear on any device, and it can be applied for any standard 3L-ANPC inverter without special requirement on the voltage rating of the inner devices. In this paper, we only focus on solution II.

C. Simulation Verification : To verify the proposed fault-tolerant strategies, simulation is implemented in MATLAB/Simulink. The simulation parameters are: dc bus voltage $V_{\mathrm{dc}} =$ 200 V, dc-link capacitors $C_1 = C_2 =$ 6.6 mF, carrier based SPWM modulation, switching frequency $f_{\mathrm{sw}} =$ 1.5 kHz, modulation index $= \mathbf{1}$, fundamental frequency $f =$ 50 Hz, and inductive load ($R = 2\ \Omega$ and $L =$ 4 mH). We assume the fault occurs and is detected at 0.05 s.

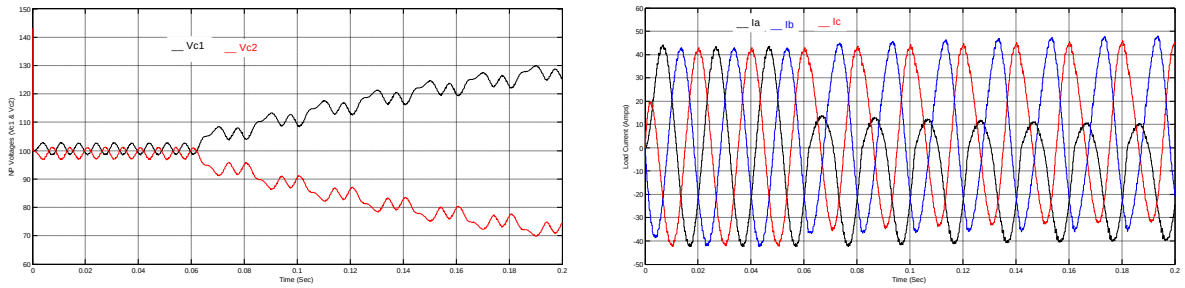

Fig. 4 (a) NP voltage and load current waveforms under S_{a1}/D_{a1} open failure (Without proposed control)

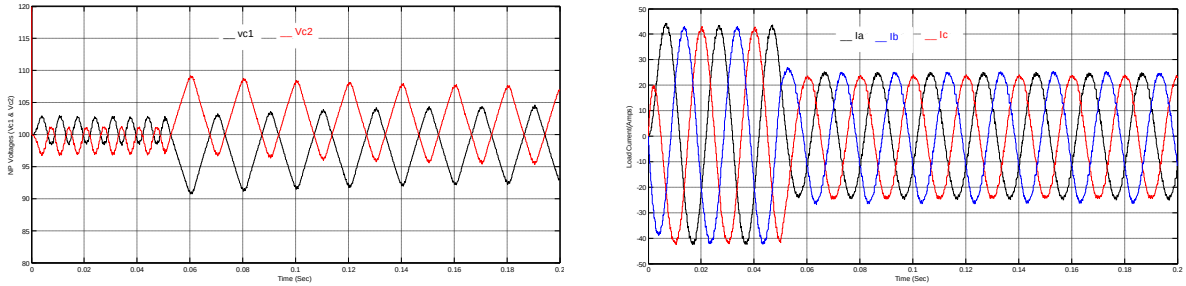

Fig. 4 (b) NP voltage and load current waveforms under $Sa1$ /$Da1$ open failure (With proposed control)

Figs. 4 and 5 show the NP voltage of dc-link and the load current waveforms without and with the proposed control for single device open failure on $S_{a\,1}$ /$D_{a\,1}$ and $S_{a\,2}$ /D_{a2} respectively.

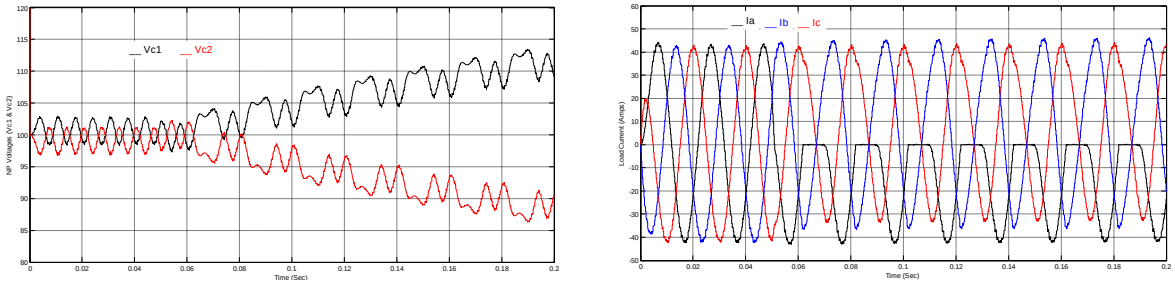

Fig. 5 (a) NP voltage and load current waveforms under $Sa2$ /$Da2$ open failure (Without proposed control)

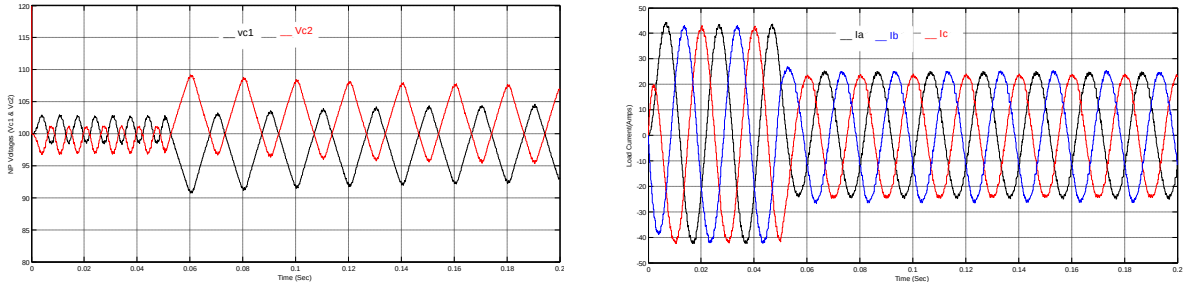

Fig. 5 (b) NP voltage and load current waveforms under $Sa2$ /$Da2$ open failure (With proposed control)

Figs. 6 and 7 show the NP voltage of dc-link and load cur- rent waveforms without and with the proposed control for single device short failure on $Sa1$ /$Da1$ and $Sa2$ /$Da2$, respectively.

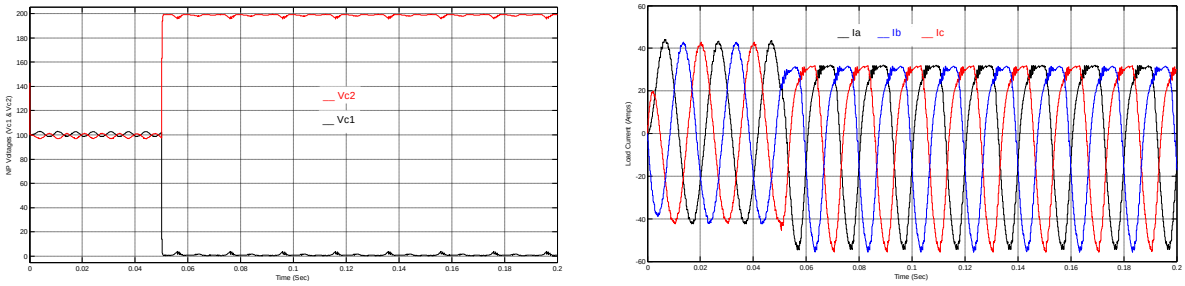

Fig. 6 (a) NP voltage and load current waveforms under $Sa1$ /$Da1$ short failure (Without proposed control)

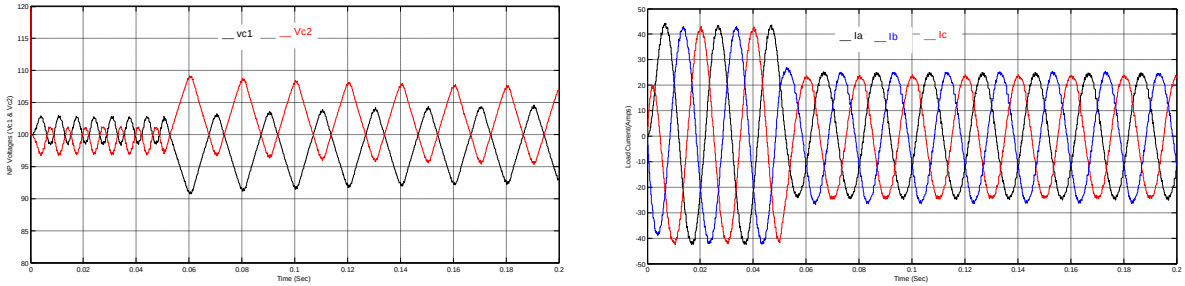

Fig. 6 (b) NP voltage and load current waveforms under $Sa1$ /$Da1$ short failure (With proposed control)

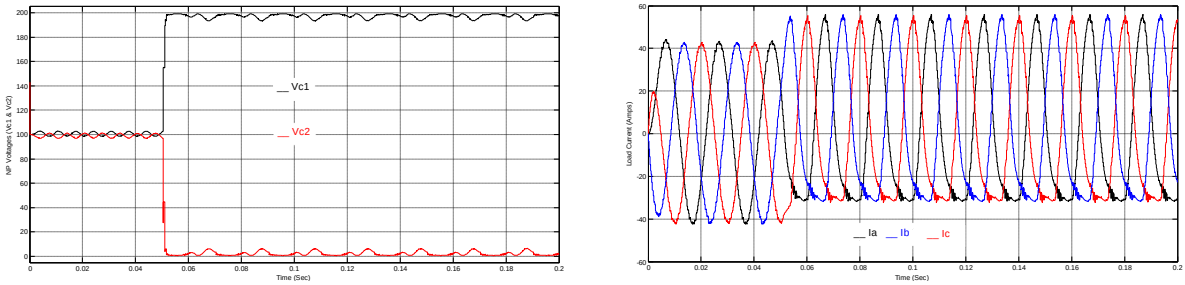

Fig. 7 (a) NP voltage and load current waveforms under $Sa2$ /$Da2$ short failure (Without proposed control)

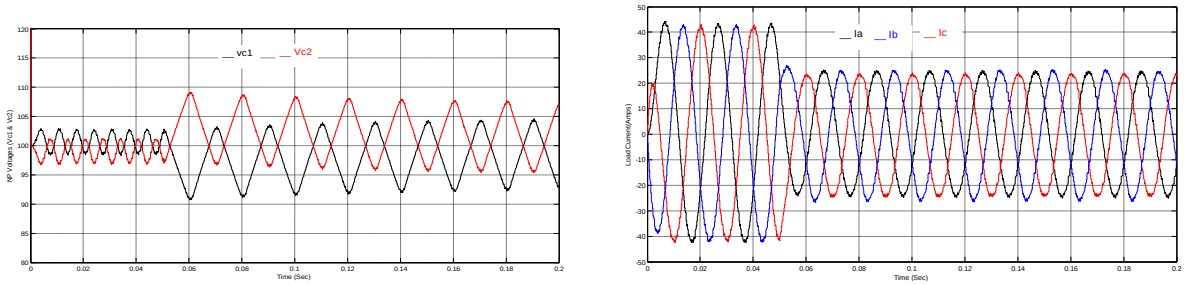

Fig. 7 (b) NP voltage and load current waveforms under $Sa2$ /$Da2$ short failure (With proposed control)

III. CONCLUSION

This paper analyzes the operation of 3L-ANPC under device failure conditions, and proposes the fault tolerant strategies to enable continuous operating of the 3L-ANPC inverters under both open- and short- failure conditions for single device failure. The analysis, simulation results show that the inverters are greatly improved by using the proposed solution. Moreover, since no additional components are added to standard 3L-ANPC inverters, the cost for robust operation of drives is lower. The results show that 3L- ANPC inverters, even though employing more semiconductor devices, have higher reliability than 3L-NPC inverters when a de-rating is allowed for the drive systems under fault tolerant operation.

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