The International Journal Of Engineering And Science (IJES)
ISSN (e): 2319 – 1813 ISSN (p): 2319 – 1805
Pages || 23-30 || 2014 ||

Modeling of New Multilevel Inverter Topology with reduced Number of Power Electronic Components

[1,]Mr.A.Vinodkumar , [2,]Mr.S.Hariprasad
[1,]*Department of Electrical and Electronics Engineering, Hyderabad Institute of Technology and Management. Hyderabad, Telangana, India.*
angothvinod@gmail.com
[2,]*Department of Electrical and Electronics Engineering, Hyderabad Institute of Technology and Management. Hyderabad, Telangana, India.*
hprasads@gmail.com

----------ABSTRACT----------
Multilevel inverters have been widely accepted for high-power high-voltage applications. Their performance is highly superior to that of conventional two-level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages. However, it has some disadvantages such as increased number of components, complex pulse width modulation control method, and voltage-balancing problem. In this paper, a new topology with a reversing-voltage component is proposed to improve the multilevel performance by compensating the disadvantages mentioned. This topology requires fewer components compared to existing inverters (particularly in higher levels) and requires fewer carrier signals and gate drives. Therefore, the overall cost and complexity are greatly reduced particularly for higher output voltage levels. A new inverter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. In the mentioned topology, the switching operation is separated into high- and low-frequency parts.

KEYWORDS *: Multilevel inverter, Reversing voltage topology, PD SPWM, Simulink, power electronics.*

I. INTRODUCTION

Multilevel power conversion was first introduced more than two decades ago. The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with the conventional power conversion approach. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce voltage (*dv/dt*) stress on the load and the electromagnetic compatibility concerns [1]. Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses. One clear disadvantage of multilevel power conversion is the higher number of semiconductor switches required. It should be pointed out that lower voltage rated switches can be used in multilevel converter and, therefore, the active semiconductor cost is not appreciably increased when compared with the two level cases.However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing [2]. To some extent, the voltage balancing can be addressed by using redundant switching states, which exist due to the high number of semiconductor devices.

Some applications for these new converters include industrial drives [3], flexible ac transmission systems (FACTS) [4]–[5], and vehicle propulsion [6], [7]. One area where multilevel converters are particularly suitable is that of renewable photovoltaic energy that efficiency and power quality are of great concerns for the researchers [12].Some new approaches have been recently suggested such as the topology utilizing low-switching-frequency high-power devices . Although the topology has some modification to reduce output voltage distortion, the general disadvantage of this method is that it has significant low-order current harmonics.

It is also unable to exactly manipulate the magnitude of output voltage due to an adopted pulse width modulation (PWM) method [8].The proposed topology is a symmetrical topology since all the values of all voltage sources are equal. However, there are asymmetrical topologies [9] which require different voltage sources. This criterion needs to arrange dc power supplies according to a specific relation between the supplies. Difference in ratings of the switches in the topology is also a major drawback of the topology. This problem also happens in similar topologies [10] while some of the high-frequency switches should approximately withstand the maximum overall voltage which makes its application limited for high-voltage products. There is another topology which requires more switches than the proposed topology for the same number of levels. Some of the proposed topologies suffer from complexities of capacitor balancing [11] This paper presents an overview of a new multilevel inverter topology named reversing voltage (RV). This topology requires less number of components compared to conventional topologies. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter.This paper describes the general multilevel inverter Schematic. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels. The simulation and experimental results of the proposed topology are also presented.

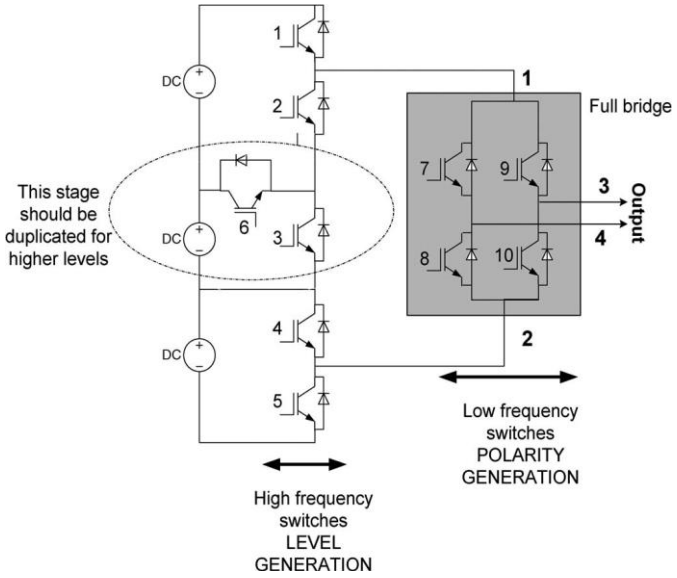

Fig.1. Schematic of a seven-level inverter in single phase.

II. NEW MULTILEVEL TOPOLOGY

A .General Description : In conventional multilevel inverters, the power semiconductors witches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generation part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability The other part is called *polarity generation* part and is responsible for generating the polarity of the output voltage which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive Levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities.The RV topology in seven levels is shown in Fig. 1. As can be seen, it requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage in Fig. 1 generates the required output levels (without polarity) and the right circuit (full-bridge converter) decides about the polarity of the output voltage. This part, which is named polarity generation, transfers the required output level to the output with the same direction or

opposite direction according to the required output polarity. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity.This topology easily extends to higher voltage levels by duplicating the middle stage as shown in Fig. 1. Therefore, This topology is modular and can be easily increased to higher Voltage levels by adding the middle stage in Fig. 1.It can also be applied for three-phase applications with the same principle. This topology uses isolated dc supplies. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. In Fig. 2, the complete three-phase inverter for seven levels is shown 3-phase system.

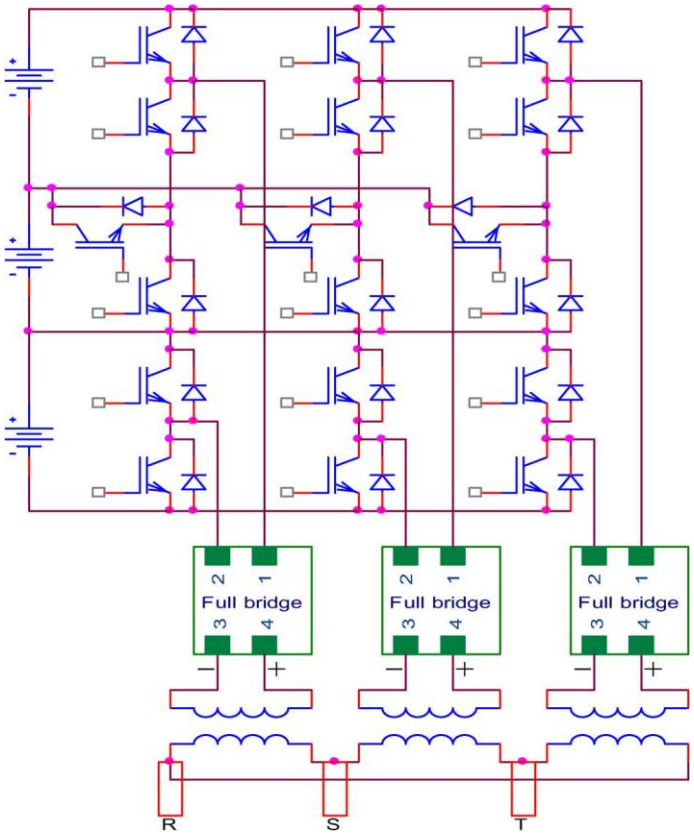

Fig 2. Three-phase RV multilevel topology

.

According to Fig. 2, the multilevel positive voltage is fed to the full-bridge converter to generate its polarity. Then, each full bridge converter will drive the primary of a transformer. The secondary of the transformer is delta (Δ) connected and can be connected to a three-phase system. This topology requires fewer components in comparison to conventional inverters. Another advantage of the topology is that it just requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists of six carriers, but in this topology, three carriers are sufficient The reason is that, according to Fig. 1, the multilevel converter works only in positive polarity and does not generate negative polarities. Therefore, it implements the multilevel inverter with a reduced number of carriers, which is a great achievement for inverter control. It is also comparable to single-carrier modulation, while this topology requires the same number of signals for PWM. However, this topology needs one modulation signal which is easier to generate as opposed to the single-carrier modulation method which needs several modulation signals [23]. Another disadvantage of this topology is that all switches should be selected from fast switches, while the proposed topology does not need fast switches for the polarity generation part.

TABLE I
SWITCHING STATES OF SEVEN LEVEL FOR RV TOPOLOGY

MODE		MULTILEVEL INVERTER SWITCHING SEQUANCE						FULLBRIDG ESWITCHING SEQUANCE			
0	+	OFF	ON	ON	ON	OFF	OFF	RB	FB	FB	RB
1	+	OFF	ON	ON	OFF	ON	OFF	RB	FB	FB	RB
	-	OFF	ON	ON	ON	OFF	OFF	FB	RB	RB	FB
2	+	OFF	ON	OFF	OFF	ON	ON	RB	FB	FB	RB
	-	OFF	ON	ON	OFF	ON	OFF	FB	RB	RB	FB
3	+	ON	OFF	OFF	OFF	ON	OFF	RB	FB	FB	RB
	-	OFF	ON	OFF	OFF	ON	ON	FB	RB	RB	FB

B. Switching Sequences : Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency component of the inverter. Then, this level is translated to negative or positive according to output voltage requirements. In Table I, the numbers show the switch according to Fig.1 should be turned on to generate the required voltage level. According to the table, there are six possible switching patterns to control the inverter. It shows the great redundancy of the topology. However, as the dc sources are externally adjustable sources (dc power supplies), there is no need for voltage balancing for this work. In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer. This will also help to decrease switching power dissipation. According to fig.1 the aforementioned suggestions, the sequences of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively. These sequences are shown in Fig. 3. As can be observed from Fig. 3, the output voltage levels are generated in this part by appropriate switching sequences. The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold. In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required as shown in Fig. 3.

In this paper, PD SPWM is adopted for its simplicity. Carriers in this method do not have any coincidence, and they have definite offset from each other. They are also in phase with each other. The modulator and three carriers for SPWM are shown in Fig. 3.

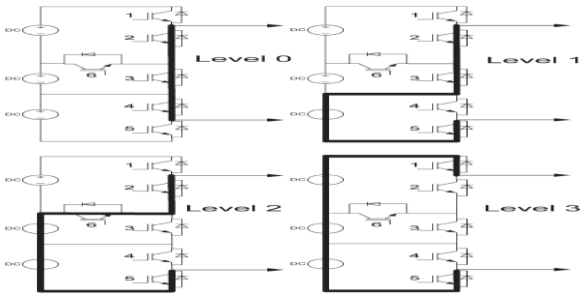

Fig.3. Switching sequences for different level generation.

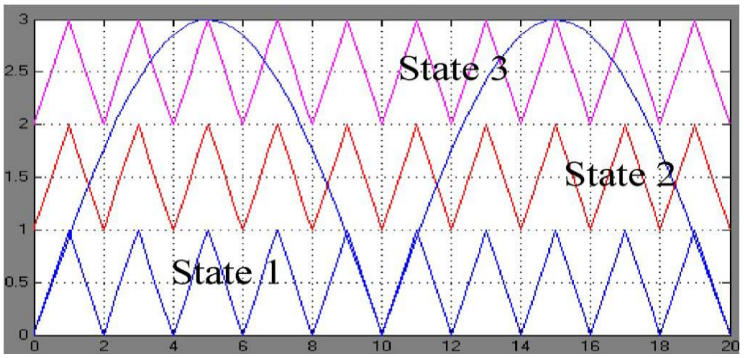

Fig.4. SPWM carrier and modulator for RV topology

According to Fig. 4, three states are considered. The first state is when the modulator signal is within the lowest carrier. The second state is is when it is within the middle carrier. Finally, the third one is when it is within. third one is when it is within the highest carrier. In each state, certain switching patterns are adopted to cover the voltage requirements. According to this definition, the switching states and switching modes are described in Table

TABLE II
SWITCHING CASES IN EACH STATE ACCORDING TO
RELATED COMPARATOR OUTPUT

STATES	**ONE**		**TWO**		**THREE**	
CAMPARE	+	-	+	-	+	-
MODE	2-3-5	2-3-4	2-5-6	2-3-5	1-5	2-5-6

Table II shows the relation between the right comparator output according to the current state and required states for switching to meet the voltage requirements. The right comparator here refers to the comparator output of the current state. As illustrated in Table II, the transition between modes in each state requires minimum commutation of switches to improve the efficiency of the inverter during switching states.
The number of switches in the path of conducting current also plays an important role in the efficiency of overall converter. For example, a seven-level cascade topology has 12 switches, and half of them, i.e., six switches, conduct the inverter current in each instance. However, the number of switches which conduct current in the proposed topology ranges from four switches (for generating level 3) to five switches conducting for other levels, while two of the switches are from the low-frequency (polarity generation) component of the inverter.
The gating signal for the output stage, which changes the polarity of the voltage, is simple. Low-frequency output stage is an H-bridge inverter and works in two modes: forward and reverse modes. In the forward mode, switches 8 and 9 as in Fig. 1 conduct, and the output voltage polarity is positive. However, switches 7 and 10 conduct in reverse mode, which will lead to negative voltage polarity in the output. Thus, the low-frequency polarity generation stage only determines the output polarity and is synchronous with the line frequency.

The resulting PWM waveforms for driving the high frequency switches in the level generation part are illustrated for one complete cycle in Fig. 5. According to Fig. 5, high frequency switches can be adopted in this stage based on the required frequency and voltage level. However, low-frequency polarity generation part drive signals are generated with the line frequency (50 Hz), and they only change at zero-voltage crossings.

TABLE III
NUMBER OF COMPONENTS FOR THREE-PHASE INVERTERS

Inverter type	**NPC**	**Flying capacitor**	**cascade**	**RV**
Main switches	6(N-1)	6(N-1)	6(N-1)	3((N-1) +4)
Main diodes	6(N-1)	6(N-1)	6(N-1)	3((N-1) +4)
Clamping diodes	3(N-1) *(N-2)	0	0	0
DC bus capacitors/ isolated supplies	(N-1)	(N-1)	3(N-1)/2	(N-1)/2
Flying capacitors	0	3/2(N-I)*(N-2)	0	0
Total numbers	(N-1) * (3N+7)	1/2(N-1)*(3N+20)	27/2(N-1)	(13N+35)/2

C. Number of Components : In the proposed converter, as can be seen, half of the switches in the full-bridge converter will not require to be switched on rapidly since they are only switched at zero crossings operating at line frequency (50 Hz). Thus, in this case, the reliability of the converter and also related expenses are highly improved. The number of required three-phase components according to output voltage levels (*N*) is illustrated. In table III [24] It can clearly be inferred that the number of components of the proposed topology is lower than that of other topologies even more so as the voltage levels increase and it will decrease tremendously with higher voltage levels. As the most important part in multilevel inverters is the power semiconductor switches which define the reliability and control complexity, the number of required switches against the required voltage level is shown fig.5 for the new topology as well as other topologies. It can clearly be inferred that the number of components of the proposed topology is lower than that of other topologies even more so as the voltage levels increase and it will decrease tremendously with higher voltage levels. Fig.6 shows the required component versus different voltages.

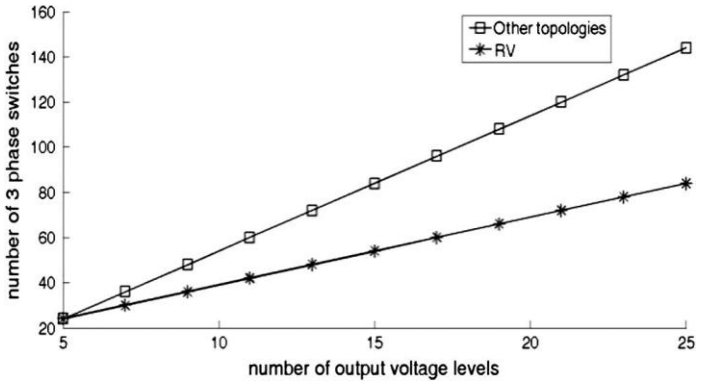

Fig.5. Required switches for multilevel inverter.

According to Figs. 5, the new topology requires fewer components and also fewer switches compared to others. Therefore, it should have the potential of finding widespread applications in high-voltage power device and apparatus that includes FACTS and HVDC. It also requires less number of components as to conventional inverters that use phase shift transformers for increasing the output voltage levels. STATCOM, which is a type of FACTS apparatus and has been widely developed in recent years, can be a good candidate for applying the topology.

III. MATLAB/SIMULINK MODELLING AND SIMULATION RESULTS

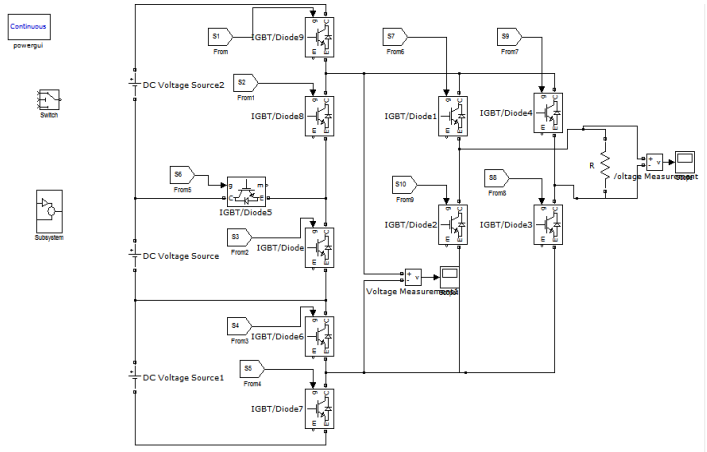

Fig.6. Simulation Circuit diagram of Single phase Seven Level Inverter

The feasibility of the proposed approach is verified using computer simulations fig.6. A model of the seven-level inverter is constructed in MATLAB-Simulink software. **A** new strategy with reduced number of switches is employed. Cascaded H bridge7 level inverter requires 12 switches to get seven level output voltage and the proposed topology requires 10 switches only. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter and can be extended to any number of levels. The schematic of the cascaded H bridge seven level inverter and proposed new seven level topology are built in MATLAB-Simulink.The topology is used to generate seven level output voltage for a single phase and three phase resistive loads shown below.

This part produces the output polarity the current output of the level generating part and output of the polarity generation part are shown. The current, which is generated by the high-frequency level generating component, is fed to the polarity generating component to define its polarity. The complete output waveform is then created, resulting in the production of the desired voltage waveform of the multilevel inverter as shown in Fig.8.The waveform of the proposed multilevel inverter with an output voltage is 600v peak-peak of a resistive load is 100 Ω is shown in Fig.7(a) The resulting output voltage THD was 18.44% , which complies with the IEEE 519 harmonic standard.

Fig.7(b) clearly show the performance of the proposed inverter for resistive loads. Therefore, this proposed topology is proven to waveform shown below. Three phase resistive load of output voltages is 800V peak-peak are shown Fig.7(b).The resulting output voltage THD was 19.51% , which is in compliance with the IEEE 519 harmonic standard

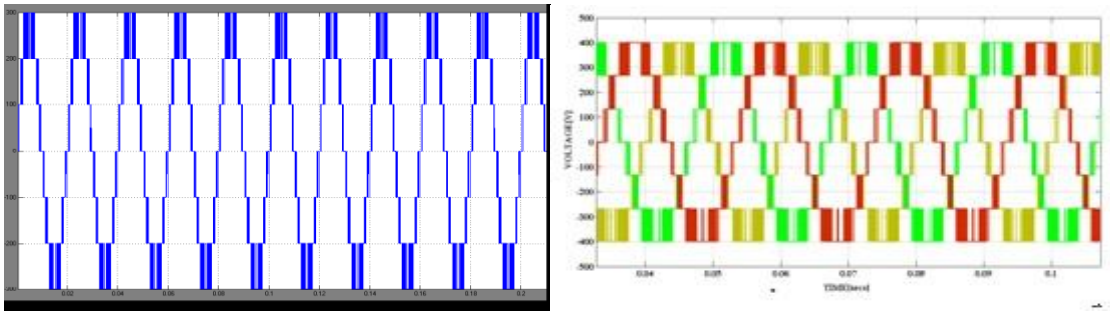

Fig.7(a) Seven level output voltage waveform for single-phase R-load (b)Seven level output voltage waveform for Three-phase R-load

IV. CONCLUSIONS

In this paper, a new inverter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the mentioned topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype.The PD-SPWM control method is used to drive the inverter. The PWM for this topology has fewer complexities since it only generates positive carriers for PWM control. The experimental results of the developed prototype for a seven-level inverter of the proposed topology are demonstrated in this paper. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of carriers for PWM.

V. FUTURE ENHANCEMENT(S)

It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the mentioned topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype.

REFERENCES

[1] K. Jang-Hwan, S.-K. Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage source inverter," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1239–1248,Jul./Aug. 2008.

[2] K. Jang-Hwan, S.-K. Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage source inverter," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1239–1248,Jul./Aug. 2008

[3] R. H. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Conf. Rec. 34th IEEE IAS Annu. Meeting*, 1999, vol. 4, pp. 2662–2669.

[4] E. Najafi and A. H. M. Yatim, "A novel current mode controller for astatic compensator utilizing Goertzel algorithm to mitigate voltage sags," *Energy Convers. Manage.*, vol. 52, no. 4, pp. 1999–2008, Apr. 2011.

[5] N. Seki and H. Uchino, "Converter configurations and switching frequenc for a GTO reactive power compensator," *IEEE Trans. Ind. Appl.*,vol. 33, no. 4, pp. 1011–1018, Jul./Aug. 1997.

[6] K. Nakata, K. Nakamura, S. Ito, and K. Jinbo, "A three-level traction inverter with IGBTs for EMU," in *Conf. Rec. IEEE IAS Annu. Meeting*,1994, vol. 1, pp. 667–672.

[7] A. Jidin, N. R. N. Idris, A. H. M. Yatim, T. Sutikno, and M. E. Elbuluk,An optimized switching strategy for quick dynamic torque control in DTC-hysteresis-based induction machines," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3391–3400, Aug. 2011.

[8] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2703–2712, Jul. 2008.

[9] E. Beser, B. Arifoglu, S. Camur, and E. K. Beser, "Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source," *J. Power Electron.*, vol. 10, no. 2, pp. 138–145, Mar. 2010.

[10] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for dc-ac conversion," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1311–1319, Sep. 2006.

[11] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M.Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE 36th Power Electron Spec. Conf.*, 2005, pp. 2296–2301.

AUTHOR PROFILE

Mr.A.Vinod Kumar was born in Telangana, India, on August 16, 1988. He received his B.Tech degree in Electrical and Electronics Engineering from ACE College of Engineering, Hyderabad ,Telangana. in 2011; currently he is pursuing Masters in Power Electronics and Electrical drives from Hyderabad institute of technology and management, Hyderabad, Telangana. His areas of interests are Power Electronics, Power systems and control systems Multilevel inverter, AC drives, and DC-DC converters.

Mr.S.Hari Prasad is currently working as Assistant professor in Hyderabad institute of technology and management, Hyderabad, Telangana. He has over 10 years of Teaching experience in the field of Electrical Engineering. His areas of Interests include Control systems, FACTS, Power Quality.