

# THD Minimisation for Phase Voltage of Multilevel Inverters Using Genetic Algorithm

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## ABSTRACT

Researchers try to enhance the efficiency and quality of the output power of multilevel inverters by use of new topologies or enhanced switching algorithms. But it should be noted that, it is not easy to change the inverter switching algorithm and doing this will increases the costs. Also these algorithms are not usually extensible to all inverter types. By considering these limitations, in this paper the THD equation of the output voltage of an asymmetric single phase cascaded multilevel inverter capable of generating 9 output voltage levels is extracted. This equation will be a function of switching angles and input voltage source values. Now, with the use of genetic algorithm which is one of the strongest optimization tools, the voltage THD is minimized and the optimized switching angles are obtained. By applying these angles in the conventional switching algorithm with fundamental frequency, the quality of the output voltage reaches its highest level. The method used in this paper is simpler than the switching algorithm changing method and can be generalized to different types of multilevel inverters. Also the use of fundamental switching frequency, will reduce switching losses. The simulation results obtained by MATLAB/SIMULINK software, confirm the performance accuracy of the proposed method.

**Keywords** - Asymmetric cascaded inverter, Genetic algorithm, Multilevel inverter, Optimization, THD.

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## I. INTRODUCTION

Today inverters are widely used in industry. For example motor drives, energy storage systems, energy production with the use of renewable energy sources and etc [1]. Therefore inverters are highly valued and researchers try to improve their output power quality. With the increase of the number of levels in the inverters output, output voltage total harmonic distortion (THD) is reduced [2]. Also the value of  $dv/dt$  is reduced [3] and this improves voltage quality. Because of this and the existence of limitations in the application of two-level inverters [4], it is recommended to use multilevel inverters in medium voltage and high power applications such as active power filters, static compensators and etc. The use of multilevel inverters also reduces switching losses [5]. These inverters are mainly divided into three types of diode clamped, flying capacitor and cascade [6]. Figure (1) shows the basic structures of these inverters [7].

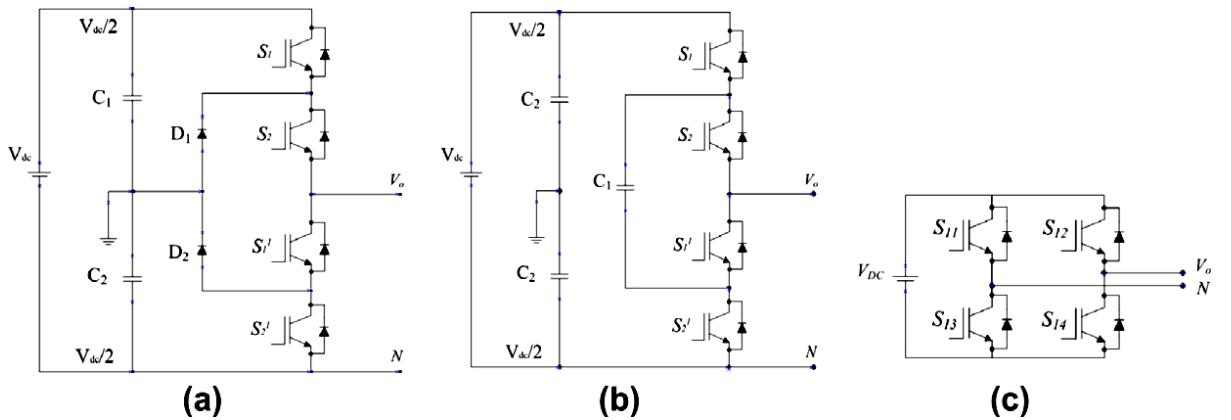
### 1.1 Diode clamped inverter

This inverter proposed by "Nabae" in 1981 [8] and actually it was a three-level inverter. The key components of this inverter are clamped diodes. For a single phase m-level diode clamped inverter, Equation (1) shows the number of DC-link capacitors ( $N_c$ ). Equation (2) shows the number of switching components ( $N_d$ ) and Equation (3) shows the number of clamped diodes ( $N_{cd}$ ).

$$N_c = m-1 \quad (1)$$

$$N_d = 2(m-1) \quad (2)$$

$$N_{cd} = 2(m-2) \quad (3)$$



**Figure 1.** Multilevel inverters. (a) Diode clamped. (b) Flying capacitor. (c) Cascade.

Diode clamped inverter is efficient in fundamental switching frequency. But using this frequency results in high output voltage and current THD and these reduce the delivery power quality. In other side, increment the number of components to increase the output voltage levels and power quality, makes the inverter bulky and increases the cost. There is an important point to use this inverter and it is the possibility of voltage imbalance of DC-link capacitors and this problem is directly related to switching angles.

### 1.2. Flying capacitor

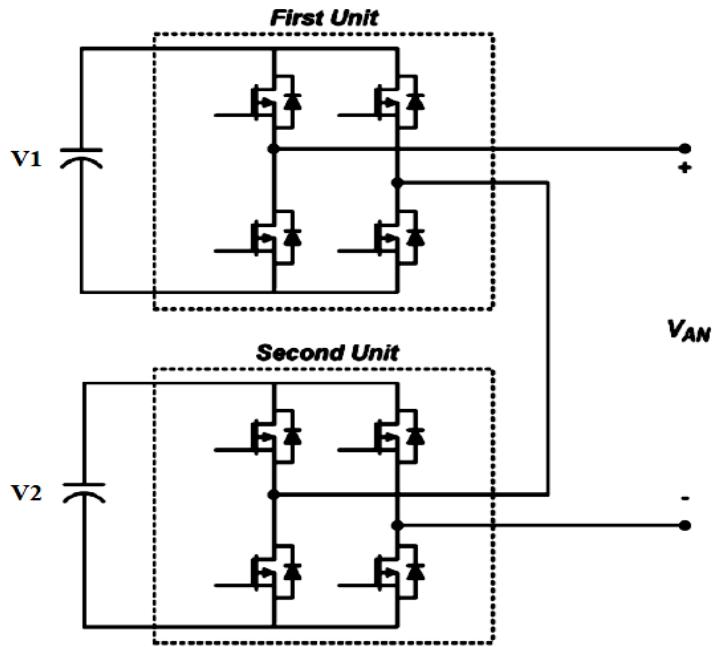
This inverter was first introduced in 1992 by "Meynard" [9]. General structure of this inverter is like diode clamped inverter but the main difference between them is that the inverter uses flying capacitors instead of clamped diodes. For a single phase m-level flying capacitor inverter, there are  $m-1$  number of DC-link capacitors and  $((m-1)(m-2))/2$  number of auxiliary capacitors. In this inverter, by increasing the output voltage levels, the accurate charging and discharging control of capacitors will be difficult and the cost and installation area will be increased.

### 1.3. Cascaded inverter

This inverter is made of series H-bridges. Each bridge is made of an input voltage source and 4 power switches and can produce 3 output voltage levels of  $+V_{DC}$ ,  $0$  and  $-V_{DC}$ . So a single phase cascaded inverter with  $m$  number of input sources needs  $4m$  number of switches. In this inverter, by increasing the number of output voltage levels, the switching components will be increased. As other way to increment the power quality, the switching frequency can be increased. But it increases the switching losses and inverter control complexity. According to above points about multilevel inverters, researchers try to increase the output power quality without significant increase in the number of inverter components and switching losses. In this paper these important points are considered and the focus is placed on cascaded inverter. This inverter has two types of symmetric and asymmetric. In symmetric mode the input voltage sources are equal and this mode can generate  $2m+1$  number of output voltage levels. Cascaded inverter can be used in asymmetrical mode. Asymmetric cascaded inverter uses input voltage sources with unequal values [10], and this reduces the number of components used in the circuit. So with the same number of components, asymmetric inverter can produce more output voltage levels than symmetric inverter and it means higher power quality. In the next section of the paper, the THD equation of the output voltage of an asymmetric single phase cascaded multilevel inverter capable of generating 9 output voltage levels will be extracted, and its value will be minimized using the genetic algorithm and optimal switching angles will be obtain.

## II. VOLTAGE THD CALCULATION

Figure (2) shows an asymmetric conventional cascaded inverter with two input voltage sources and 8 unidirectional power switches with antiparallel diode to supply inductive loads.



**Figure 2.** Single phase asymmetric conventional cascaded inverter with two sources.

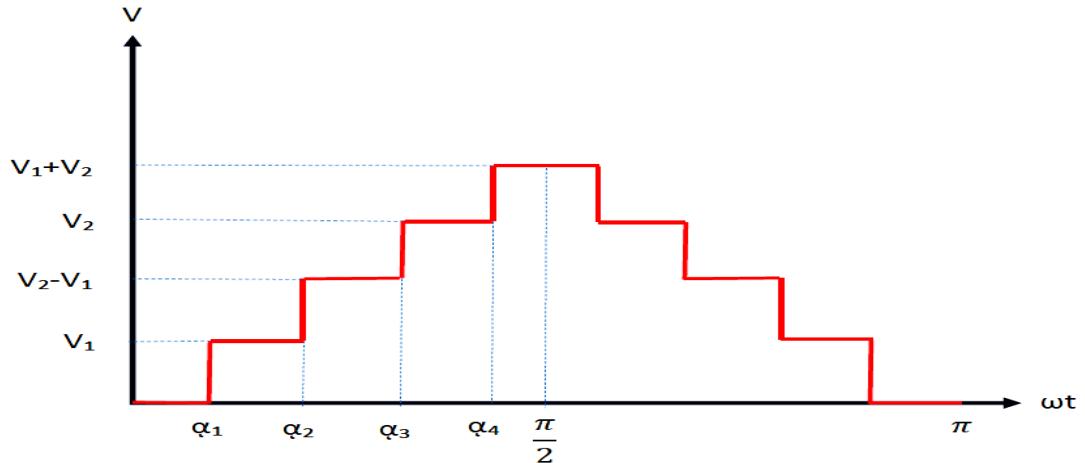
If  $n$  number of sources exist in the input side of a conventional cascaded inverter, then Equation (4) will show the maximum obtainable voltage levels for the output. Of course, the maximum number of levels can only be generated when the input voltage sources are used with proper coefficients. Sources with trinary coefficient are usually selected for this purpose. In trinary incremental scheme the values of input sources are:  $V_1=1\text{p.u.}$ ,  $V_2=3\text{p.u.}$ ,  $V_3=9\text{p.u.}$ ,  $V_4=27\text{p.u}$  and so on.

$$N_{\text{level}} = 3^n \quad (4)$$

In Figure (2), if input sources values satisfy Equation (5), then this inverter can generate 9 levels at the output voltage.

$$V_2 > 2 \times V_1 \quad (5)$$

Figure (3) shows a symbolic half cycle form of output voltage of shown inverter in Figure (2). Switching angles and input source values can be seen in this figure. The voltage THD formula is obtained from Equation (6). According to this equation, to calculate THD, Fourier series should be obtained. The Fourier series of this voltage waveform can be written according to Equation (7). The expression for amplitude of all harmonic components of the phase voltage, is given as Equation (8). By using this equation, to obtain  $V_{1\text{rms}}$  that is the RMS value of fundamental component, Equation (9) should be used.  $V_{\text{rms}}$  is the RMS value for the output voltage waveform that can be obtain through Equation (10). Now with the use of equation just mentioned, the  $V_{\text{rms}}$  for voltage waveform shown in Figure (3) can be seen in Equation (11). With the use of Equations (9) and (11) and by placing them in Equation (6), the THD calculation formula is completed. Now with the use of genetic algorithm and by considering one condition of  $(0 < q_1 < q_2 < q_3 < q_4 < \pi/2)$ , and by use of trinary incremental scheme for input voltage values, the THD equation can be optimized and the minimum value can be obtained for it. The optimization results are given in Table (1). This table shows the optimized value for switching angles with fundamental frequency. By using any other of switching angles to switching in fundamental frequency, the THD value can not be minimised. for example Table (2), shows two non-optimized selection groups for switching angle values. As it is clear from this table, the value of output voltage THD is not at the minimum value.



**Figure 3.** Half cycle output voltage of asymmetric 9 levels conventional inverter.

$$\text{THD} = \sqrt{\left(\frac{V_{\text{rms}}^2}{V_1^2(\text{rms})}\right) - 1} \quad (6)$$

$$V_{\text{phase}}(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \quad (7)$$

$$V_n = \frac{4}{n\pi} (V_1 \cos(n\alpha_1) + (V_2 - 2V_1) \cos(n\alpha_2) + V_1 \cos(n\alpha_3) + V_1 \cos(n\alpha_4)) \quad \text{for odd } n \quad (8)$$

$$V_{1\text{rms}} = \frac{V_1}{\sqrt{2}} = \left(\frac{2\sqrt{2}}{\pi}\right) (V_1 \cos \alpha_1 + (V_2 - 2V_1) \cos \alpha_2 + V_1 \cos \alpha_3 + V_1 \cos \alpha_4) \quad (9)$$

$$V_{\text{rms}} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} V^2(\omega t) d\omega t} \quad (10)$$

$$V_{\text{rms}} = \sqrt{\left(\frac{2}{\pi}\right) \left( V_1^2(\alpha_2 - \alpha_1) + (V_2 - V_1)^2(\alpha_3 - \alpha_2) + V_2^2(\alpha_4 - \alpha_3) + (V_2 + V_1)^2\left(\frac{\pi}{2} - \alpha_4\right) \right)} \quad (11)$$

**Table 1.** Optimum switching angles and minimum value of voltage THD.

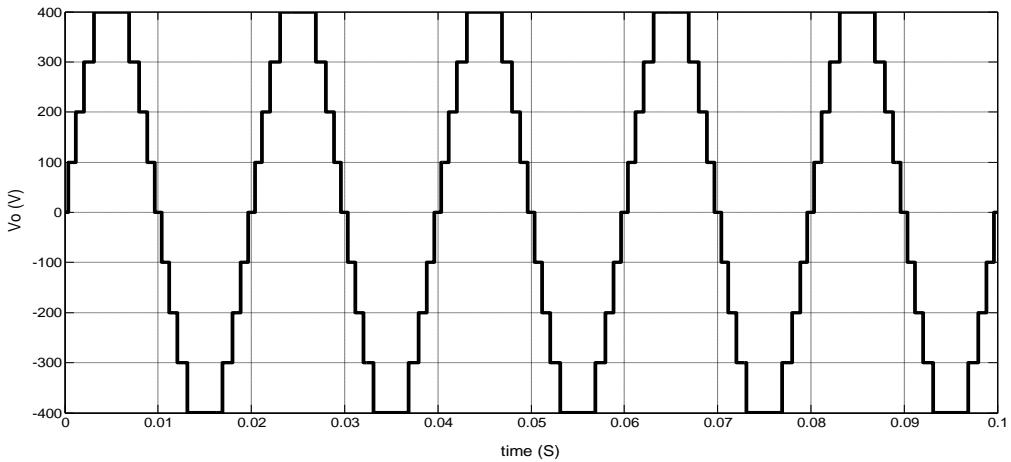
THD(%)	V <sub>1</sub> (v)	V <sub>2</sub> (v)	α <sub>1</sub> (degree)	α <sub>2</sub> (degree)	α <sub>3</sub> (degree)	α <sub>4</sub> (degree)
8.9	100	300	6.760	20.741	36.210	55.806

**Table 2.** Non-optimum switching angles and non-minimum value of voltage THD.

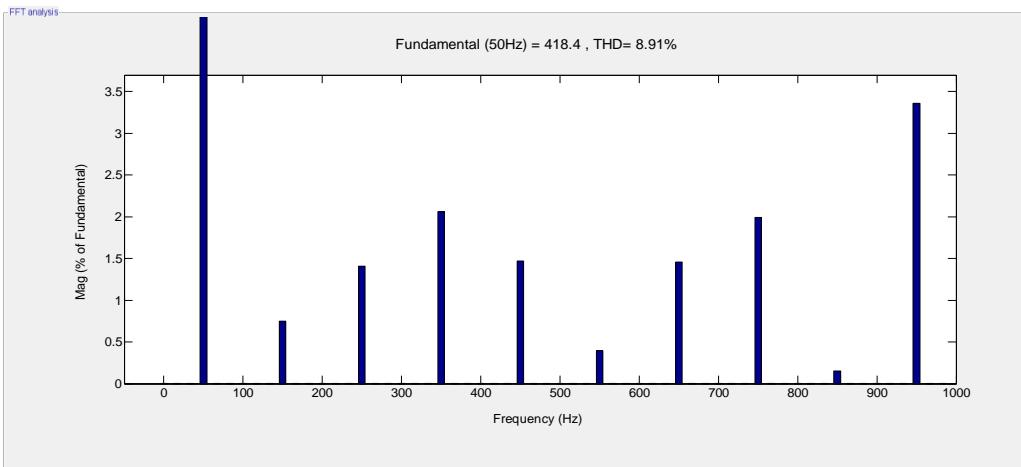
No	THD (%)	V <sub>1</sub> (v)	V <sub>2</sub> (v)	α <sub>1</sub> (degree)	α <sub>2</sub> (degree)	α <sub>3</sub> (degree)	α <sub>4</sub> (degree)
1	15.52	100	300	15	30	45	60
2	22.05	100	300	18	36	54	72

### III. SIMULATION RESULTS

In this section, the inverter shown in Figure (2) is simulated based on the values shown in Table (1) with the use of MATLAB/SIMULINK software. The inverter load is considered in an ohmic form with a value of  $R=15\Omega$ . Figure (4) shows the output voltage and Figure (5) shows the harmonic spectrum and the value of the voltage waveform THD. As can be seen from these figures, the simulation results confirm the validation of the proposed method advantages and its theoretical operation and control scheme.



**Figure 4.** Output voltage of asymmetric 9-level conventional inverter by using Table (1) data.



**Figure 5.** Output voltage THD and harmonic spectrum.

### IV. CONCLUSION

In this paper, for a 9-level cascaded inverter, optimized switching angles are obtained with the use of genetic algorithm and the THD equation. The use of these values in switching, minimized voltage THD. This method can be extended to various types of multilevel inverters and is simpler and cheaper compared to new switching methods.

## References

- [1] Honglin Zhou, Shuai Xiao, Geng Yang and Hua Geng, "Modeling and Control for a Bidirectional Buck-Boost Cascade Inverter," *IEEE TRANSACTIONS ON POWER ELECTRONICS*, VOL. 27, NO. 3, pp. 1401-1413, 2012.
- [2] Won-Kyun Choi and Feel-soon Kang, "H-bridge based Multilevel Inverter using PWM Switching Function," in Proc. INTELEC, pp. 1-5, 2009.
- [3] A.R. Beig and A. Dekka, "Experimental verification of multilevel inverter-based standalone power supply for low-voltage and low-power applications," *IET Power Electron.*, Vol. 5, Iss. 6, pp. 635–643, 2012.
- [4] Jin Wang and Damoun Ahmadi, "A Precise and Practical Harmonic Elimination Method for Multilevel Inverters," *IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS*, VOL. 46, NO. 2, pp. 857-865, 2010.
- [5] P. Palanivel and S.S. Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," *IET Power Electron.*, Vol. 4, Iss. 8, pp. 951–958, 2011.
- [6] Dioge A. B. Zambra, Cassiano Rech and José Renes Pinheiro, "Comparison of Neutral-Point-Clamped, Symmetrical, and Hybrid Asymmetrical Multilevel Inverters," *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS*, VOL. 57, NO. 7, pp. 2297-2306, 2010.
- [7] Ilhami Colak, Ersan Kabalci and Ramazan Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Elsevier Journal of Energy Conversion and Management*, Vol 52, pp. 1114–1128, 2011.
- [8] Nabae A, Takashi I and Akagi H, "A new neutral-point clamped PWM inverter," *IEEE Trans Ind Appl*, Vol 17, pp. 518–23.1981.
- [9] Meynard TA and Foch H, "Multi-level conversion: high voltage choppers and voltage-source inverters," In: *Proceedings of IEEE power electronics specialists conference*, Toledo (Spain); 1992.
- [10] Javier Pereda and Juan Dixon, "High-Frequency Link: A Solution for Using Only One DC Source in Asymmetric Cascaded Multilevel Inverters," *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS*, VOL. 58, NO. 9, pp. 3884-3892, 2011.