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Design and Physical Implementation of Asymmetric 8T-SRAM Memory Systems

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ABSTRACT
Low power and high speed requirement is a challenging task in the design of SRAM memory systems. In this paper two types of 8T-SRAM cells are presented with incorporation of high-Vt transistors at appropriate locations to achieve both dynamic and static power minimization and data stability without disturbing its performance. These 8T-SRAM Cells are designed and simulated using Cadence design tool for 90nm CMOS process technology. The two cells are compared for power dissipation and have power dissipation lower than standard 6T-SRAM cell. Stack 8T-SRAM cell with high-Vt has lower power consumption than dual port 8T-SRAM cell with high-Vt by 2.6 times for dynamic power dissipation, and 15 times for static power dissipation. For 64bit system, compared to dual port 8T-SRAM cells without high-Vt transistors , total power reduced by 11.8 times and 8T-SRAM cell with high-Vt transistors reduced by12.5 times.

KEYWORDS : *data stability, dual Vt SRAM, Low power SRAM.*

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I. INTRODUCTION

Present day workstations, low-power processors, computers and super computers are using fast SRAMs and will require larger density memories with faster access time. High-density, low-power SRAMs are needed for applications such as hand-held terminals, laptops, notebooks and IC memory cards, due to the fact that these systems frequently use battery as power source and hence it should consume power as low as possible. It is also necessary for maintaining low cooling and packing costs for these systems. The power dissipation reduction in SRAMs can be achieved not only by power supply voltage reduction, but also using low-power circuit techniques. An SRAM cell must be designed such that it provides a non-destructive read operation and a reliable write operation. These two requirements impose contradicting requirements on SRAM cell transistor sizing. In this work asymmetric 8T-SRAM cell is implemented with judicial incorporation of high-Vt and low-Vt transistors to achieve low power at good performance [1].

II. EXISTING METHODS FOR POWER MINIMIZATION

In this section two different existing 8T-SRAM memory cells are presented.

2.1.AN 8T-SRAM CELL WITH IMPROVED STABILITY

The fundamental stability problem in 6T cells is that in the read condition, a pass-gate pulls the "0" storage node up to a nonzero value. Adding two FETs to a 6T cell provides a read mechanism that does not disturb the internal nodes of the cell shown in fig.1, thereby eliminating the worst-case stability condition. This requires separate read and write word lines and can accommodate dual-port operation with separate read and write bit lines. Without read disturbs, the worst-case stability condition for an 8T cell is that for two cross-coupled inverters, which provides a significantly larger SNM [2].

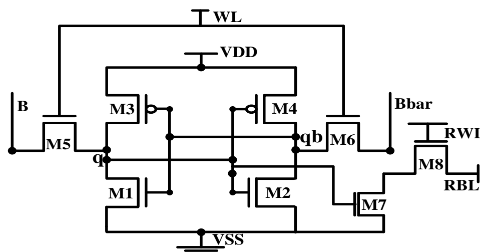

Fig.1: Dual Port 8T-SRAM Cell

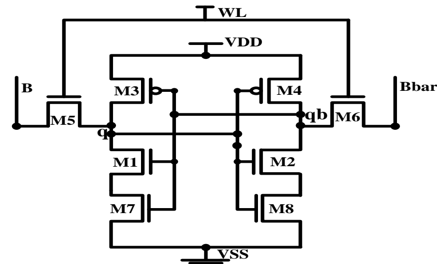

Fig.2: Stack 8T-SRAM Cell

2.2.Ultra Low Power 8T SRAM Cell

The 8T SRAM shown in fig.2 is an extension of 6T-SRAM with two additional NMOS transistors M7 and M8, one each in pull down path of cross coupled inverters, used to achieve leakage power reduction. The access transistors are connected to the word line at their respective gate terminals, and the bit-lines at their drain terminals. The word line is used to select the cell while the bit lines are used to perform write and read operations on the cell. Internally, the cell holds the stored value on one node and its complement on the other node. The node ‘q’ holds the stored value while other node ‘qb’ holds its complement. The two complementary bit lines are used to improve speed of write and read operations [3].

III. PROPOSED ASYMMETRIC 8T-SRAM CELLS WITH HVT TRANSISTORS

The SRAM cells shown in fig.1 and fig.2 both make use of 8 transistors. SRAM of fig.1 requires two additional control signals RBL and RWL. In addition to WL where as SRAM of fig.2 requires only word line as control signal. These two cells are evaluated for their power consumption. Further High-Vt transistors are incorporated in appropriate locations in order to achieve still better power reduction. The SRAM cells of fig.1 and fig.2 modified by using high-Vt transistors are shown in fig.3 and fig.4.The use of dual-threshold voltages for power reduction has been examined. In both the methods, all the transistors in the circuit are initially set to have a low threshold voltage. Subsequently, the threshold voltage of some of the gates that do not lie on critical paths is increased. The leakage power can be reduced by up to 50% without affecting the performance of the circuit. In this work the effects of dual threshold voltage dual-threshold voltage selection scheme on the dynamic power dissipation of a given circuit is considered. High-Vt transistors are also used with regular transistors to reduce the total power dissipation without sacrificing much of speed.

IV. DUAL PORT 8T-SRAM CELL

The 8T memory cell shown in Fig.3 has a separate read port comprised of two transistors. The two separate read and write word lines can accommodate dual-port operation with separate read and write bit lines.

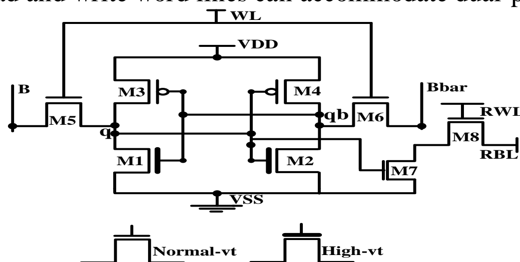

Fig 3: Dual Port 8T-SRAM With Hvt

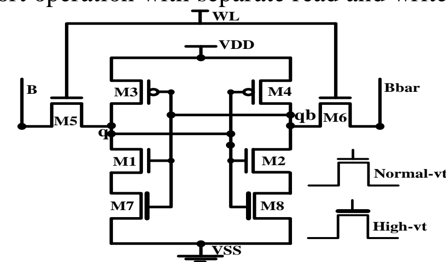

Fig.4: Stack 8T-SRAM With Hvt

3.1.STACK 8T-SRAM

The 8T SRAM cell consists of two cross-coupled inverters made up of transistors M1, M3 and M2, M4. The transistors M5, M6 are access transistors. The two additional NMOS transistors M7 and M8 are taken as Hvt transistors, one each in pull down path of cross coupled inverters, used to achieve leakage power reduction. The access transistors are connected to the word line at their respective gate terminals, and the bit-lines at their drain terminals. The word line is used to select the cell while the bit lines are used to perform write and read operations on the cell. Internally, the cell holds the stored value on one node and its complement on the other node. The node ‘q’ holds the stored value while other node ‘qb’ holds its complement. The two complementary bit lines are used to improve speed of write and read operations [3].

The two asymmetric cells proposed in this work are tested for functionality and performance in one bit system, 4X4 array, 8X8 array. The read and write operations of the memory system are performed by using appropriate peripheral units. The complete system is shown in fig 5.

3.2.THE SRAM MEMORY SYSTEM ARCHITECTURE

The fig 5 shows block diagram of 64-bit 8T-SRAM system which consists of write circuit, precharge, 8T-SRAMs Sense amplifier and 3:8 decoder. The individual blocks are explained further.

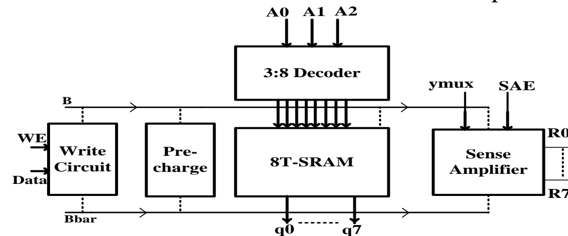

Fig. 5: Block Diagram of 64-Bit 8T-SRAM

3.3.WRITE CIRCUIT

The data write circuit consists of two inverters and four NMOS transistors. The write circuitry when activated by write enabled signal (WE) writes data and its complement onto the bit-lines. The data and its complement are written onto the individual nodes ‘q’ and ‘qb’ of the selected word through the access transistors of the SRAM cell. For every column of array one write circuit is used [5].

3.4.PRECHARGE

The pre-charge circuit consists of three PMOS transistors with the single command signal PRE. Transistors PM1 and PM2 connect the bit lines with the VDD source for the pull-up. Transistor PM3 connects the two bit lines for their equalization. In many cases, when one of the two bit lines is already at VDD, PM3 helps the pull-up of the other bit line. In the memory structure there is a pre-charge circuit for each couple B/Bbar, as observed in the simplified block diagram in fig.5. In the normal operation of the memory, the pre-charge circuit is most of the time activated and its action is to set the voltage level of each of bit lines at a certain value, VDD for most of memories [4].

3.5.SENSE AMPLIFIER

Sense amplifiers are very susceptible to differential noise on bit lines, and they detect small voltage differences. If bit lines are not pre charged, residual voltages on lines from the previous read may cause failure in the output. In this work the differential sense amplifier is used, based on an analog differential pair and no clock is used. During read operation the sense amplifier enable (SAE) signal is applied to the sense amplifier as shown in fig. 5. This activates the sense amplifier for read operation only for Short period of time. At the same time the column is isolated from the bit-lines by using signal Ymux. It causes one of the bit-lines B/Bbar to discharge from the precharged value. This creates a differential voltage on the bit-lines which is sensed by the sense amplifier and amplified to the full extent. The outputs of sense amplifier are reflected as R0 and RB0.

3.6.ECODER

In this work two types of decoders are used, 2:4 decoder, and 3:8 decoder for 4X4 system and 8X8 system respectively. The Lyon-Schediwy decoder[5] is used as it uses minimum number of transistors compare to other decoders. In ‘Lyon-Schediwy decoder’ is viewed as 2^n n-input NOR gates sharing PMOS pull-ups. The 4 words are selected by 2:4 decoder and 8 words are selected by 3:8 decoder. The address bits A_1A_0 and $A_2A_1A_0$ determine the word to be selected for data write or read operation. Only one wordline is activated in any given time. The 4 selection lines WL_0 to WL_3 are connected to 4rows of 4x4 and 8 selection lines WL_0 to WL_7 for are connected to 8 rows of the 8x8 memory array.

V. SIMULATION RESULTS

The proposed circuits are simulated in Cadence Virtuoso tool in 90nm technology process. A comparison of the Access Time, Static and Total Power Dissipation of the Dual Port 8T-SRAM cell with Stack 8T-SRAM cell are presented in Table. 1. and comparison of the Access Time, Static and Total Power Dissipation in the Dual Port Hvt 8T-SRAM cell with Stack Hvt 8T-SRAM cell are presented in Table.2. The power dissipation for different 8T-SRAM systems with and without high-Vt transistors given in Table 3.

The output waveforms of single cell 8T-SRAM, 4x4 8T-SRAM system and 8X8 8T-SRAM system are shown in fig.6, fig.7 and fig.8 respectively.

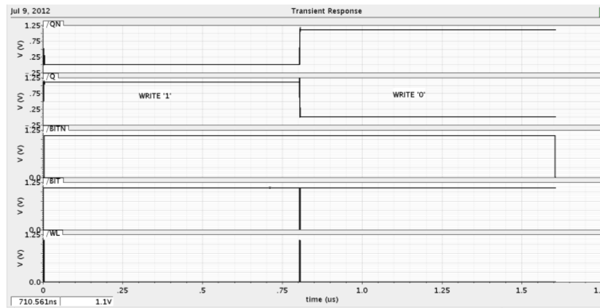

Fig 6: Simulated Output Of Single 8T-SRAM Cell

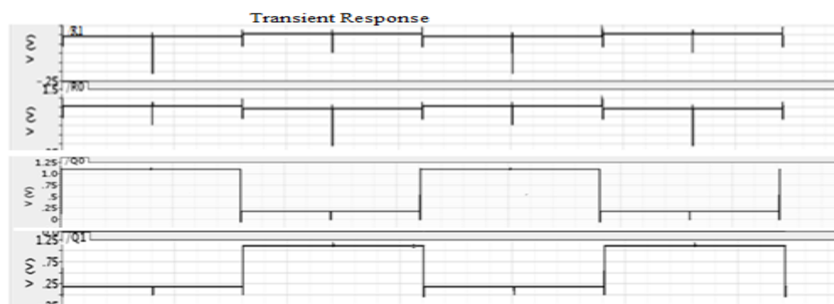

Fig.7:Output Waveform for data q and read r for 16bit 8T-SRAM Cell

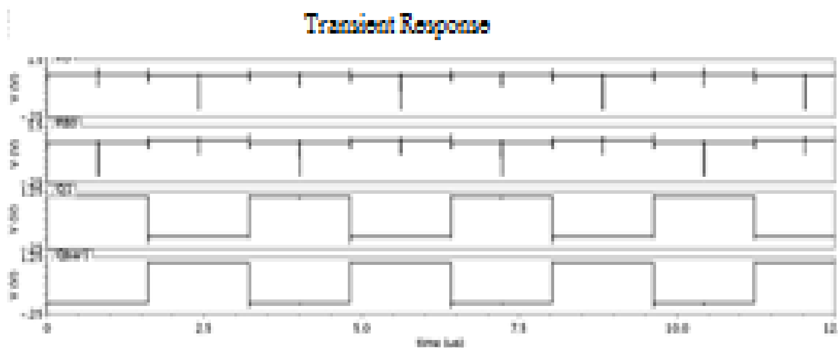

Fig .8: Output Waveform for data q and read r for 16bit 8T-SRAM Cell

The output waveforms of 8T-SRAM cell for storage node q and qb, and output r and rb are shown in fig.7. and fig.8 for 16 bit and 64 bit respectively. which shows only two samples i.e. q0,qb0,and r0,rb0, similarly we will get six more sets of outputs.

Table 1: Static, Total Power Dissipation and Access Time for Single 8T-SRAM Cell without Hvt (VDD=1.1)

SINGLE SRAM CELL WITHOUT HIGH-VT	STATIC POWER IN NANO W			TOTAL POWER IN NANO W	ACCESS TIME (PECO SEC)	
	WRITE1	WRITE0	HOLD		WRITE 1	WRITE 0
DUAL PORT 8T-SRAM	39.0	38.53	38.64	74.17	22.78	26.44
STACK 8T-SRAM	2.676	2.676	2.685	28.41	25.25	27.92

Table 2: Static, Total Power Dissipation and Access Time for Single 8T-SRAM Cell with Hvt (VDD=1.1V)

SINGLE SRAM CELL WITH HIGH-VT	STATIC POWER IN NANO W			TOTAL POWER IN NANO W	ACCESS TIME (PECO SEC)	
	WRITE1	WRITE0	HOLD		WRITE 1	WRITE 0
DUAL PORT 8T-SRAM	1.165	1.163	1.166	22.10	22.79	26.42
STACK 8T-SRAM	1.366	1.366	1.366	18.54	25.07	29.17

Table 3: Total Power Dissipation 8T-SRAMsyatem with and without Hvt (VDD=1.1V)

TOTAL POWER IN W	8T-SRAM WITHOUT HIGH-VT		8T-SRAM WITH HIGH-VT	
	4X4	8X8	4X4	8X8
DUAL PORT 8T-SRAM	1.24E-3	23.55E-3	1.22E-6	22.76E-3
STACK 8T-SRAM	793.7E-6	1.99E-3	661.8E-6	1.81E-3

VI. CONCLUSION

The effectiveness of high-Vt transistors and the reduction of leakage power is studied in this work. esign choices.In this paper twudied in this work.o different types of 8T-SRAM cells with high-Vt are designed , Reduction of both dynamic and static power effectively is observed. All simulations are done using Cadence design process for 90nm technology.

REFERENCES

[1] Sunil Kumar Ojha. Dr. P.R. Vaya. Department of E.C.E. Department of E.C.E. Amrita School of Engineering."*Novel Architecture of SRAM Cell for Low-. Power Application*"

[2] Chang, L.; Fried, D.M.; Hergenrother, J.; Sleight, J.W.; Dennard, R.H.; Montoye, R.K.; Sekaric, Lidija; Mcnab, S.J.; Topol, A.W.; Adams, C.D.; Guarini, K.W.; Haensch, W., "Stable SRAM cell design for the 32 nm node and beyond," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on* , vol., no., pp.128,129, 14-16 June 2005.

[3] Ravi Kumar. K. I, Vijayalaxmi. C. Kalal, Rajani. H. P, Dr. S. Y. Kulkarni. "*Design and Verification of Low Power 64bit SRAM System using 8T SRAM:Back-End Approach*" . International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2012.

[4] Luigi Dilillo, Patrick Girard Serge, Pravossoudovitch, Arnaud Virazel. "Analysis and Test of Resistive-Open Defects in SRAM Pre-Charge Circuits"JETTA – Special issue on ETS'2005

[5] Neil H. E. Weste David Harris Ayan Banerjee, CMOS VLSI Design (Third edition,2005).

[6] DAN CLEIN " CMOS IC LAYOUT"Concepts, Methodologies, and Tools,1999.

[7] Douglas A.Pucknell Kamran Eshraghian" Basic VLSI Cesign"Third Edition.1994.

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