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Comparison and Simulation of Full Bridge and LCL-T Buck DC-DC Converter Systems

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----------**Abstract**----------
The DC-DC Converter topologies have received increasing attention in recent years for Low power and high performance applications. The advantages DC-DC buck converters includes increased efficiency, reduced size, reduced EMI, faster transient response and improved reliability. The front end LCL-T in a buck converter is connected in sequence manner to improve the electrical performances and to reduce the switching losses. It futures several merits such as multi output capability and also will associate with one or two capacitors so has to improve resonant operations. This paper compares conventional buck converter and LCL-T type converter designed for low voltage and low power applications and simulation results are compared for both converters.

Keywords - *DC-DC Converter, Buck converter, LCL-T type converter and Full-Bridge Converter*

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I. INTRODUCTION

IN CONVENTIONAL full-bridge converters, the four switches must sustain the input voltage when they are "off." In applications using high values of input voltage, such as railway traction, that voltage can be larger than the safe operating voltage of power transistors that the designer would like to use, if it would be possible. A straightforward way to meet the requirements is to use transistors with sufficiently high breakdown voltage, with the disadvantages of higher cost and higher "on" resistance than would be the case if the transistors could be rated for operation at (for example) half of that voltage.

In a previous approach [1], each switch was realized as two transistors in series, with voltage-balancing components that would cause the two transistors to share the voltage equally. Then each transistor would sustain only half of input voltage. This approach worked well, but the equipment cost had to include the cost of eight power transistors for the full-bridge, and the voltage-balancing components. The circuit configuration for full-bridge converter is shown in Fig 1.

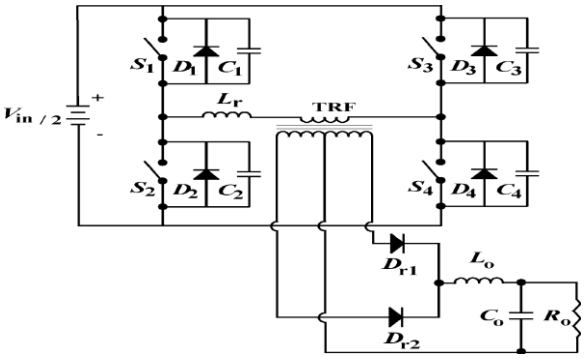

Fig.1. Conventional full-bridge converter

In the new approach proposed here, shown in Fig. 2, the two legs of the full bridge (each leg containing the usual two switches in series) are connected in series across the supply voltage. The node at which the two legs are joined is held at half of the input voltage, by bypass/filter capacitors that are connected to each of the two input rails. (This adds one more bypass capacitor to the usual input bypassing.) As in many present-day full-bridge converters, e.g., [2], this topology can be operated with

a) Capacitive turn-off snubbing to reduce turn-off switching power losses;

b) Resonant transitions that provide zero-voltage turn-on to eliminate turn-on switching power losses.

II. LCL-T BUCK CONVERTER.

The proposed converter is derived from the conventional full bridge topology presented in Fig. 1. Therefore, several operation characteristics of the full-bridge converter are also presented by the proposed structure. Fig. 2 shows the power-stage circuit. The upper leg comprises switches S_1 and S_2; and the lower leg comprises switches S_3 and S_4. The example design that was built and simulated (Section III) use metal oxide semiconductor field effect transistor (MOSFET) switches. In each MOSFET switch, the internal substrate diode conducts inverse- polarity current and clamps the switch reverse voltage at about -1 V. (If bipolar junction transistors are used, external anti-parallel diodes should be added.) The MOSFET internal C_{oss} capacitances are used asC_1- C_4, providing capacitive turn-off snubbing. In some applications (but not in the example in Section III), the internal capacitances can be supplemented with external capacitors that should be connected across the switches with as low wiring inductance as possible [4].

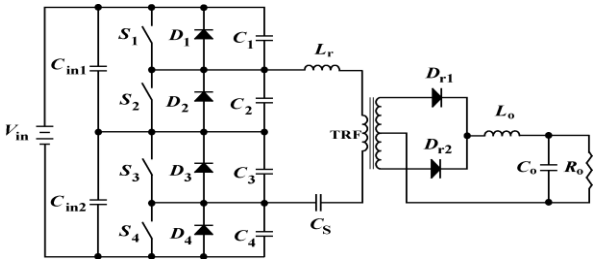

Fig. 2. The proposed LCL-T Buck converter

The input capacitors $C_{in1}$and C_{in2} bypass the input voltage and generate a bypassed dc mid-point voltage of $V_{in}/2$. As the switches go through their cycle of switching, to be discussed below, each switch has $V_{in}/2$ applied across it while it is "off." C_s is a dc-blocking capacitor that blocks the dc voltage of $V_{in}/2$ from being applied to the series combination of Lr and TRF. In this application, C_s is large enough to act as only a dc voltage source, to prevent dc current from flowing through L_r and TRF. If a resonant load network is used C_s can be the series-connected resonance capacitor [5]. The stored energy in L_r charges and discharges the snubbing capacitors C_1 – C_4 during a conduction gap that is provided between turning-off one of a pair of switches and turning-on the other switch of the pair. That action brings the switch voltage to zero before the switch is turned-on. L_r comprises the sum of an external inductor and the internal primary-side leakage inductance of the transformer. The transformer provides galvanic isolation and voltage transformation, between the source and the load R_o. DR_1 and DR_2 rectify the rectangular-wave output of the transformer, and L_o and C_o filter-out the ripple in the rectified output.

From the waveforms of proposed LCL-T type buckconverter of Fig. 3, note that the maximum voltages $V_{in}/2$ across the "off" switches are only because the join-point of $C_{in1}$and C_{in2} is at voltage $V_{in}/2$: the voltage across S_1 or S_2 is the voltage on C_{in1} , and the voltage across S_3 or S_4 is the voltage on C_{in2} , but both of those capacitovoltages are $V_{in}/2$.

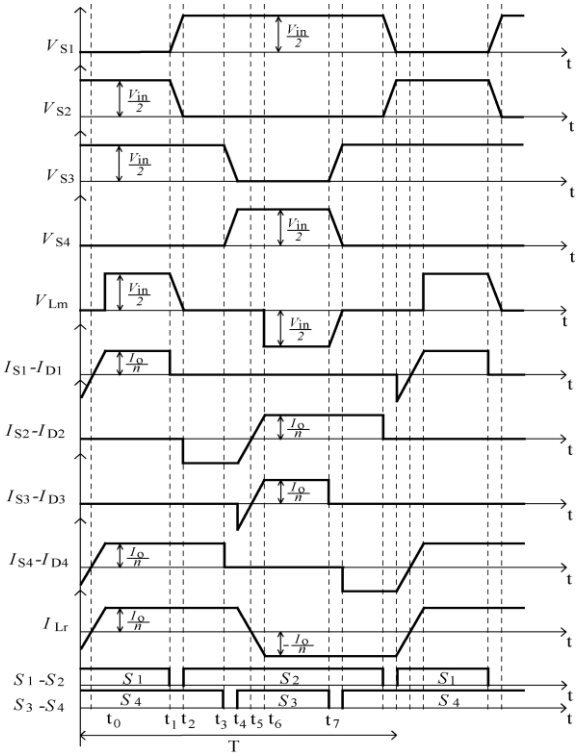

Fig. 3. Waveforms of LCL-T type Buck Converter

The principle of operation is analyzed adopting ideal conditions, but some considerations must be done in a practical application.

The input capacitors $C_{in1}$and C_{in2} are charged and discharged during the free-wheeling period, which occurs in the stage 3 and in its equivalent stage at the second half-period of operation. The voltage in these capacitors can be different from $V_{in}/2$ if the switch-timing sequence of the switches has asymmetry. However, a special control circuit is not necessary, because, as verified in the practical implementation, a very large asymmetry is needed to cause a significant difference from the ideal voltage value of $V_{in}/2$.

The ideal value of the series capacitor voltage V_{cs} is also $V_{in}/2$. During the first operation stage this capacitor receives energy from the input source and after the sixth stage this energy is transferred to the load. This capacitor is designed considering a low voltage ripple (5%–10%), operating as a voltage source. But at the converter start-up, this capacitor is discharged (Vcs. =0) Thus, while V_{cs} the does not reach $V_{in}/2$, the transformer demagnetization

will not occur correctly. But, as the capacitance of the series capacitor is small, V_{cs} the voltage changes quickly and in some switching cycles reaches the ideal value. Classical current protection circuits can avoid an eventual excessive switch peak current during this transition.

B. Turn-On and Turn-Off Switching

Turn-off: The commutation process of the proposed converter is similar to the classical ZVS PWM full-bridge converter. The turn-off losses are reduced by the action of the snubber capacitors that are in parallel with the switches. When a switch is turned-off, the switch current flows through the commutation capacitor, charging this capacitor. Thus, the capacitor voltage, which is also the switch voltage, rises progressively until it reaches V_{cin} the voltage. Therefore, the crossing of the voltage and current in the switch is reduced and the turn-off losses are minimized.

Turn-on: The converter uses zero-voltage turn-on to eliminate the turn-on switching losses. The zero-voltage turn-on of the switches is particularly important for converters operating at high dc input voltage, because the power dissipated in switching at nonzero voltage goes as the square of the dc input voltage. The active switches are turned on while the anti-parallel diodes are conducting, so the switches turn-on at essentially zero voltage and almost zero current. But turn-on losses occur if the turn-off snubber capacitors are not fully discharged. Switches S_3 and S_4 turn-off in the power-transfer stage (stage 1 in Section III), and the output current referred to the primary accomplishes the charge and discharge of the snubber capacitors (linearly with time). The large stored energy of the ripple-filter inductor L_o is available for this purpose, so, as a practical matter, S_{23} and S_4 and will always be turned-on at zero voltage.

But switches S_3 and S_4 turn-off in the free-wheeling stage during which the transformer is short circuited by the output rectifier. Thus, only the energy stored in the circuit inductance L_x (that includes the transformer primary- side leakage inductance) is available to charge and discharge the snubber capacitors, in a resonant way. The minimum current that maintains zero-voltage turn-on for S_1 or S_3 is

$$I_{\min} = \frac{V_{in}}{2} \cdot \sqrt{\frac{2.C}{L_r}}$$

where C is the snubber capacitor $C = C_1 = C_2 = C_3 = C_4$.

A larger value of L_r decreases the primary-side current needed to obtain zero-voltage turn-on of $S_1$and S_3, but the inductance of the resonant inductor L_r is limited by the maximum allowed reduction of duty ratio [8].

III. Simulation Reults

Four switched LCL-T buck dc-dc converter is shown in Figure 5.the input dc voltage is rectified into high switching AC frequencies using four switches LCL-T buck inverter. Switching pulses are given to S_1&S_4, S2&S_3 are shown in Figures 6&7 and also their input voltages, output voltage &output current are shown in Figures 7&8. The dc output voltage is variation at 600V. The variation of output with decrease input is shown in Figure 9.

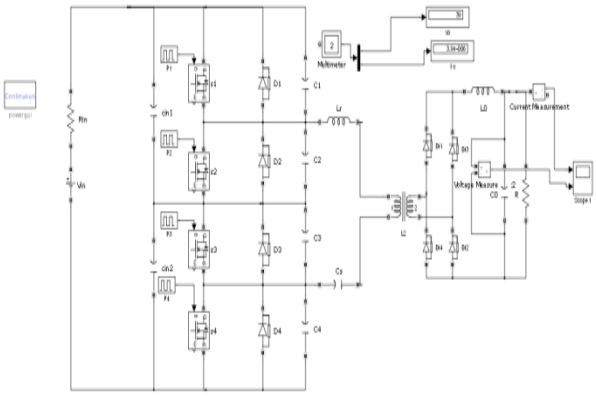

Fig. 5.Simulation of the proposed converter

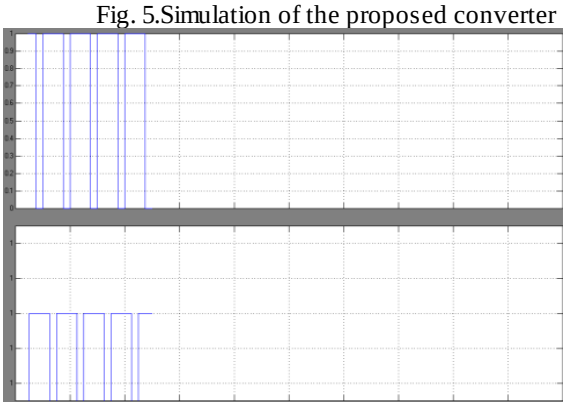

Fig. 6. Driving pulses of S_1 &S_2

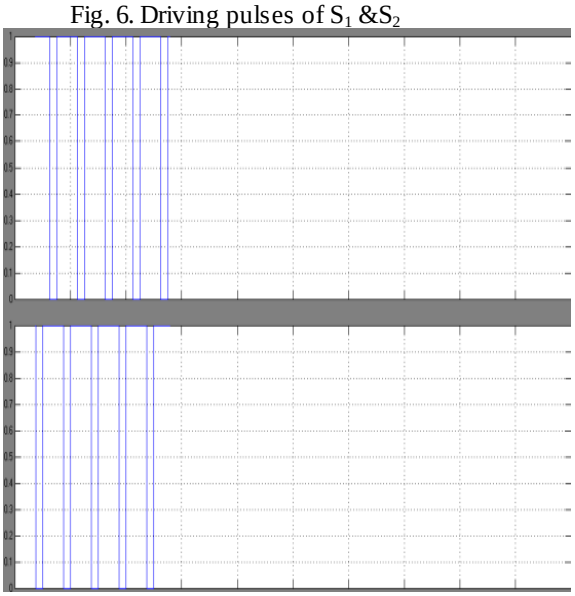

Fig. 7. Driving pulses of S_3 & S_4

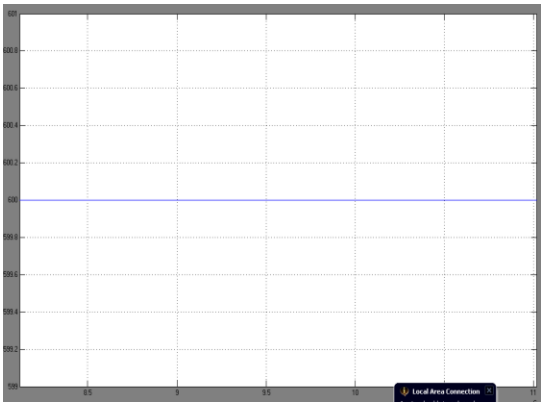

Fig.8 Inputvoltage

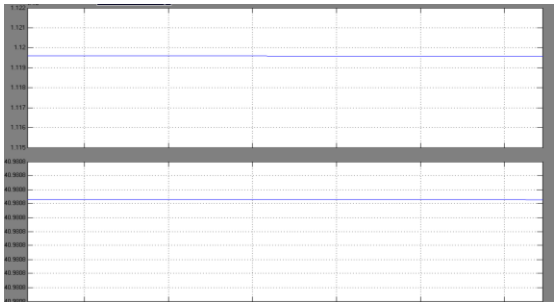

Fig.9 output voltage &output current

Vin	Input Power		Output Power		Efficiency	
	Conv	Prosd	Conv	Prosd	Conv	Prosd
70	570	2135	495	1900	86.84	88.99
60	416	1568	361	1394	86.78	88.90
50	290	1100	251	969	86.55	88.90
40	185	702	159	617	85.95	87.90

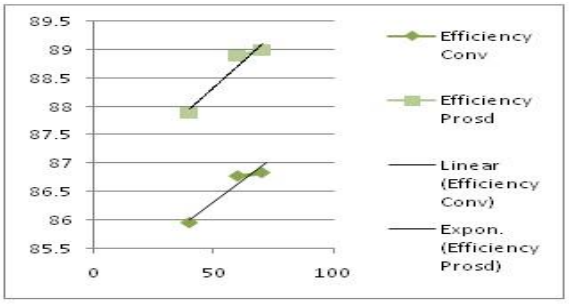

Fig 10. Efficiency of Conventional and proposed methods

From Figure 10 it is observed that the efficiency of the conventional full bridge buck converter has been improved by implementing proposed LCL-T type buck converter.

IV. CONCLUSION

The proposed four switch LCL-T buck dc-dc converter system is simulated using MATLAB/Simulink and the results are presented. The proposed converter system acquires constant voltage. And it is observed the switching losses have been reduced and the converter output efficiency is more than that of conventional full bridge buck converter. This four switch LCL-T power circuit topology is well suited to its economical realization.

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