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Design of High Speed Multiplier for Digital FIR Filter using Ancient Urdhava Tiryagbhyam Techniques

M.Sivasankar, (M.E-A.E)., G.Nanjappan,M.E.,
Student/Dept of Applied Electronics,
Jayam College of Engineering and Technology, Dharmapuri DT, India.
Assistant Professor/ECE Dept,
Jayam College of Engineering and Technology, Dharmapuri DT, India.

----------**ABSTRACT**----------
The high speed multiplication operation plays a important part in Digital Signal Processor (DSPs). The FIR filter is also called as convolution filter since convolution is the fundamental concept of designing Finite Impulse Response filter. Vedic mathematics is the ancient mathematics which consists of 16 sutras. The use of multiplier with higher speed is of utmost importance to any DSP. The proposed method of multiplier is based on Vedic multiplication sutras. Vedic multiplication based on Urdhava Tiryagbhyam (vertically and crosswise) sutra. This algorithm is applied to digital arithmetic and multiplier architecture. The coding is simulating using Verilog and synthesis is done using Xilinx ISE 9.2i series. This Urdhava Tiryagbhyam multiplier can bring about great improvement in DSP performance.

KEYWORDS- Urdhava Tiryagbhyam, Vedic Multiplier, Verilog, FIR.

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. The Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions (CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as, Fast Fourier Transform(FFT), convolution, filtering and in microprocessors in its arithmetic and logic unit . Since multiplication dominates the execution time of most algorithms (DSP), so there is a need of high speed multiplier in DSP. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

The High speed multiplier is one of the most important components in designing Digital Signal Processors (DSPs). Digital Signal Processing (DSP) operations such as convolution, correlation, Fast Fourier Transforms (FFTs) etc make use of multipliers. Computational speed and execution time are the two factors that decide the efficiency of multiplication algorithm. In DSP, filtering is a common term that is applied to various applications. Digital video require digital filters to reduce noise due to coding and transmission through a noisy channel.

In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, and area and power consumption.

The multiplier is a fairly large block of a computing system. The amount of circuitry involved is directly proportional to the square of its resolution i.e. a multiplier of size n bits has n2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time; multiplier is not only a high delay block but also a major source of power dissipation.

In algorithmic and structural levels, a lot of multiplication techniques had been developed to enhance the efficiency of the multiplier; which encounters the reduction of the partial products and/or the methods for their partial products addition, but the principle behind multiplication was same in all cases. Vedic arithmetic is the ancient system of Indian mathematics which has a unique technique of calculations based on 16 Sutras (Formulae). "Urdhava Tiryagbhyam" is a Sanskrit word means vertically and crosswise formula is used for smaller number multiplication. Conventional multiplication is a technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. It is the standard technique used in chip design, and provides significant improvements over the "long multiplication" technique.

Vedic multipliers are based on Vedic Sutras. In Sanskrit word 'Veda' stands for 'knowledge'. Vedic mathematics is believed to be reconstructed from Vedas by Sri Bharti Krishna Tirathaji between the years 1911 to 1918. The Vedic mathematics has been divided into sixteen different Sutras which can be applied to any branch of mathematics like algebra, trigonometry, geometry etc. Its methods reduce the complex calculations into simpler ones because they are based on methods similar to working of human mind thereby making them easier. It has been seen that being coherent and symmetrical, they consume lesser power and acquire lower chip area. Designs based on Vedic Mathematics have been used in many applications like ALU, MAC etc. and have shown better results.

The main objectives are,

i. To reduces the time delay and power consumption.
ii. To reduce the 40-60% of processing time by using Vedic multiplier.
iii. To improve the speed of process.
iv. To increase the efficiency

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications.

II. PROPOSED SYSTEM

I proposed to design a Vedic multiplier for digital FIR filter using Vedic mathematics. It is an ancient mathematics which has a unique technique of mental calculation with the help of simple rules and principles based on 16 sutras. One of the sutra is Urdhava Tiryagbhyam. This algorithm is applied to digital arithmetic and multiplier architecture is formulated. The coding is done using Verilog and synthesis is done using Xilinx ISE series. This Vedic multiplier can bring about great improvement in DSP performance. The advantages are

i. Urdhava-Tiryagbhyam reduces the area, time delay and power consumption.
ii. It reduces the 40-60% of propagating time by using Vedic multiplier.
iii. It improves the speed of process.
iv. Provide a better efficiency than conventional method.

III. FIR FILTER

The direct form realization of FIR filter can be obtained by using linear convolution. Consider FIR filter having impulse response h (n) as represented in Figure 1

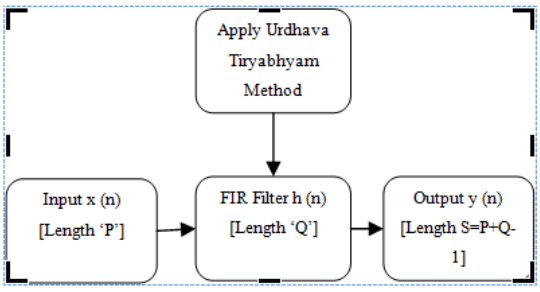

Fig 1: Basic block diagram of FIR filter

Let x (n) = Input sequence having length 'P'.
x (n) = {0, 1, 2, . , P . 1}
h (n) = impulse response of filter having length 'Q'.
h (n) = {0, 1, 2, . , Q . 1}
The linear convolution of x (n) and h (n) produces the output sequence y (n) and the length of y (n) is

$$S = P + Q-1 \qquad (1)$$

The length of x (n) and h (n) can be made equal to 'S' by adding required number of zeros in x (n) and h (n). This is known as zero padding. It means we have to increase the length of x (n) by P points and length of h (n) by Q points to make the total length 'S = P + Q-1'.

In FIR filter, both the sequences x (n) and h (n) are finite, so linear convolution will be finite. The convolution having input x of length P with filter h of length Q will give the output sequence y (n).

$$y(x) = \sum_{k=0}^{Q-1}(\mathrm{h(k)} \times (n-k)) \qquad (2)$$

Figure (2) represents direct form structure of FIR filter. By expanding equation (2) we can draw the direct form structure of FIR filter.

$$y(n) = h(0)x(n) + h(1)x(n-1) + h(2)x(n-2) + h(3)x(n-3) + \ldots\ldots + h(Q-1)x(n-Q+1) \quad (3)$$

The direct form realization structure is also called canonic structure since the number of delay elements in the block diagram is equal to the order of difference equation of a digital filter. The figure (2) contain 'Q-1', delay blocks. This structure has 'Q-1', additions and 'Q' multiplications.

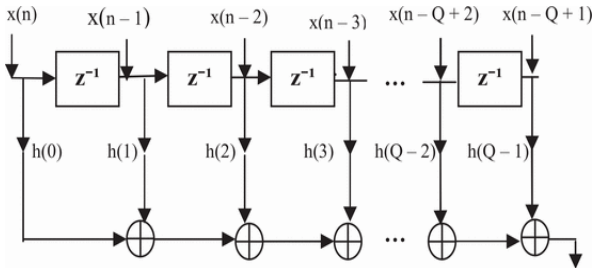

Fig 2: Direct form structure of FIR system

IV. VEDIC MATHEMATICS

Vedic mathematics is an ancient mathematics that has a unique system of computation based on simple rule and basic principles with which mathematical problem can be solved. It deals with many modern mathematical terms including arithmetic, trigonometry, geometry (plane, co-ordinate), quadratic equations, factorization and even calculus. The beauty of Vedic mathematics lies in the fact that it reduces the complex looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles and sutra on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884–1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swami-ji constructed 16 sutras (formula) and 16 Upa sutras (sub formula) after extensive research in Atharva Veda. These formulae are not to be found in present book of Atharva Veda because these formulae were constructed by Swami-ji himself.

Vedic mathematics is not only a mathematical wonder but also it is logical. That's why Vedic Mathematics has such a degree of eminence which cannot be disapproved. Due to these phenomenal characteristic, Vedic Mathematics has already crossed the boundaries of India and has become a leading research topic in abroad. Vedic Mathematics deals with several simple as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful.

The word 'Vedic' is a Sanskrit word derived from the word 'Veda' which means the collection of all knowledge. From the ancient times Vedas were passed from previous generation to next generation orally rather than written. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc.

These Sutra's meanings with few words are enlisted below alphabetically:

1. (Anurupye) Shunyamanyat - If one is in ratio, the other is zero.
2. Chalana-Kalanabyham - Differences and Similarities.
3. Ekadhikina Purvena - By one more than the previous one.
4. Ekanyunena Purvena - By one less than the previous one.
5. Gunakasamuchyah - The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah - The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah - All from 9 and last from 10.
8. Parvarya yojayet - Transpose and adjust.
9. Puranapuranabhyam - By the completion or no completion.
10. Sankalana-vyavakalanabhyam - By addition and by subtraction.
11. Shesanyankena Charamena - The remainders by the last digit.
12. Shunyam Saamyasamuccaye - When the sum is the same that sum is zero
13. Sopaantyadvayamantyam - The ultimate and twice the penultimate.
14. Urdhava-tiryagbhyam - Vertically and crosswise.
15. Vyashtisamanstih - Part and Whole.
16. Yaavadunam - Whatever the extent of its deficiency.

The Sub Sutras are

1. Anurupyena
2. Shishyate Sheshsamjnah
3. Adyamadye Nantyamantyena
4. Kevalaih Saptakam Gunyat
5. Vestanam
6. Yavadunam Tavadunam
7. Yavadunam Tavadunikutya Varganka ch Yojayet
8. Antyayordhshakepi
9. Antyatoreva
10. Samucchayagunitah
11. Lopanasthapanabhyam
12. Vilokanam

V. URDHAVA TIRYAGBHYAM

Urdhava Tiryagbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. Urdhava Tiryagbhyam is Sanskrit word which means "Vertically and crosswise". The multiplication is based on an algorithm called Urdhava Tiryagbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. The Urdhava Tiryagbhyam is always function for even number of sequence and gives odd number of sequences. Urdhava Tiryagbhyam sutra is also known as array multiplication technique.

It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhava Triyagbhyam. Multiplication technique plays important role in designing of FIR filter. This sutra can be generalized for any N×N bit multiplication. Figure 3 illustrates the line diagram for the multiplication using Urdhava Tiryagbhyam method.

Now for example if we have FIR filter of order 4 with input sequence x(n) = [1, 2, 3, 4] and filter coefficient h(n) = [30, 342, 45, 6], then output sequence y(n) of FIR filter is given by

y(0) = 1*30 = 30
y(1) = 1*342 + 2*30 = 402
y(2) = 1*45 + 2*342 + 3*30 = 819
y(3) = 1*6 + 2*45 + 3*342 + 4*30 = 1242
y(4) = 2*6 + 3*45 + 4*342 = 1515
y(5) = 3*6 + 4*45 = 198
y(6) = 4*6 = 24

y(n) = [30, 402, 819, 1242, 1515, 198, 24]

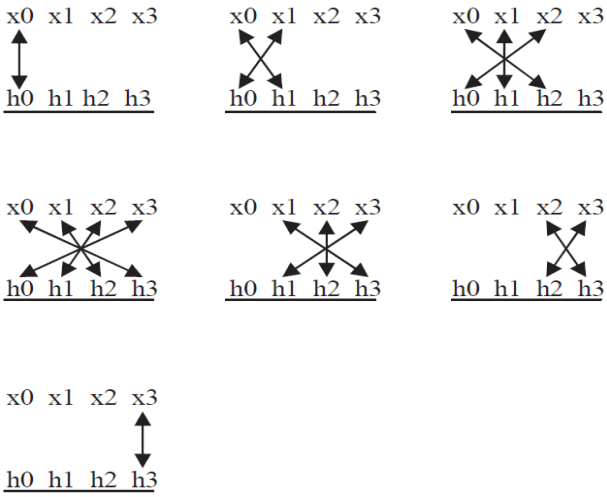

Fig. 3: Multiplying two numbers using Urdhava Tiryagbhyam method

2-Bit Vedic multiplier

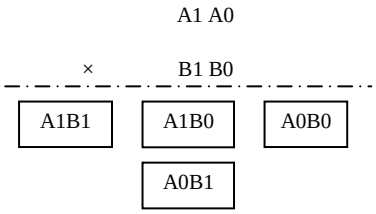

Fig 4: Sample Presentation for 2-Bit Vedic Multiplication

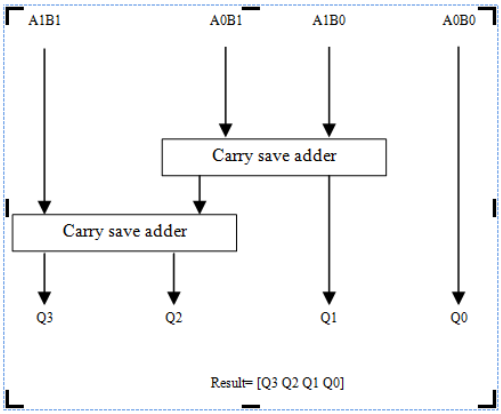

Fig 5: Block Diagram of 2-Bit Vedic Multiplier

8-Bit Vedic multiplier

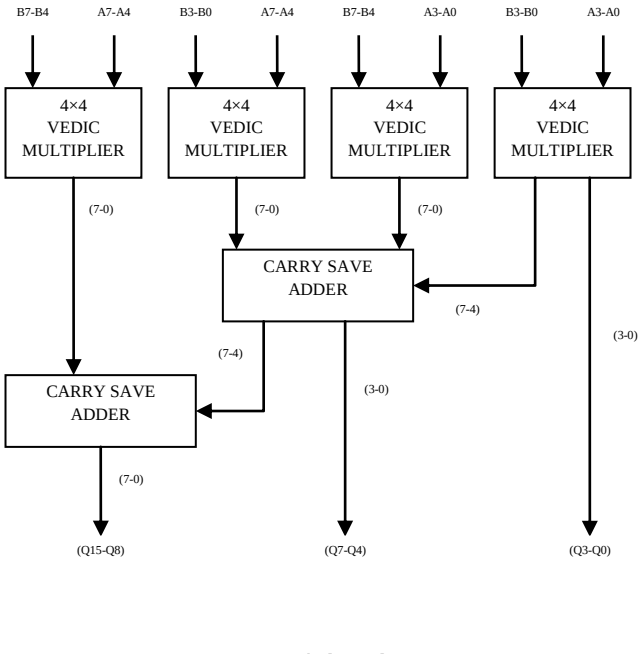

Fig 6: Block Diagram of 8-Bit Vedic Multiplier

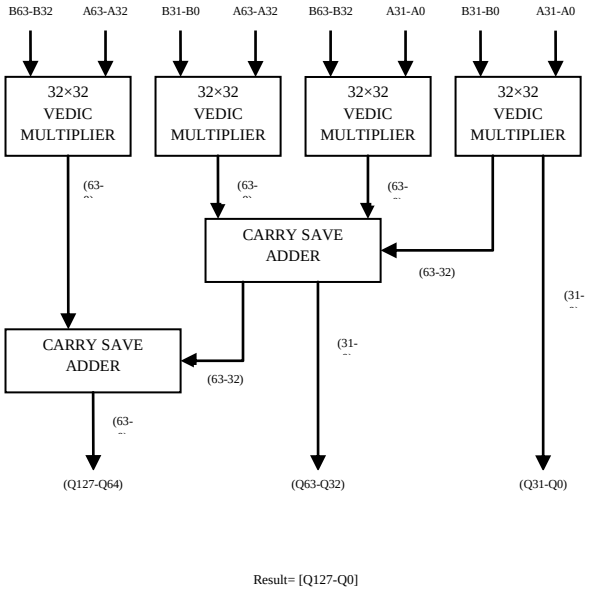

Fig 7: Block Diagram of 64-Bit Vedic Multiplier

Multipliers	Array Multiplier(ns)	Vedic Multiplier(ns)
4-Bit	13.582	12.657
8-Bit	26.564	18.506
16-Bit	55.430	24.823
32-Bit	110.348	31.750
64-Bit	220.184	40.332

Fig 8: Timing analysis using Xilinx

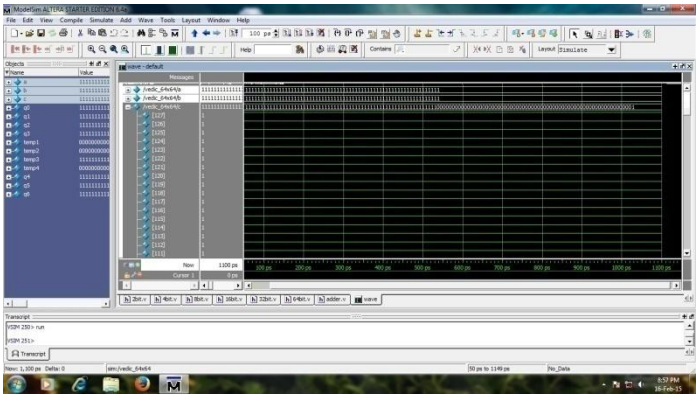

Fig 9: Output waveform for 64 bit Vedic multiplier

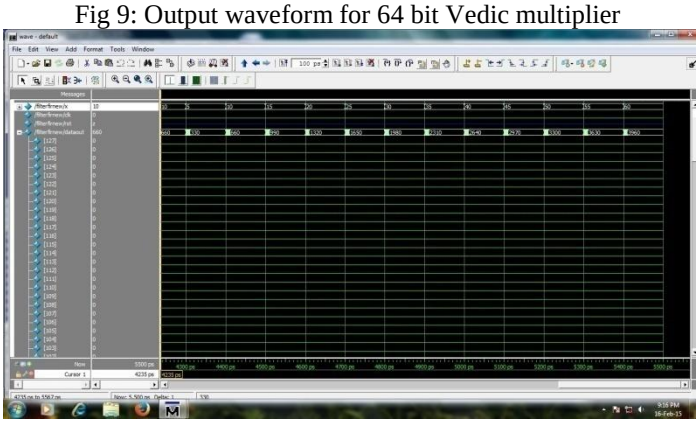

Fig 10: Output waveform for 11 tap FIR filter using 64 bit multiplier

VI. CONCLUSION

The design for FIR filter based on Vedic multiplication sutras. Vedic multiplication is based on Urdhava Tiryagbhyam (vertically and crosswise) sutra. This algorithm is applied to digital arithmetic and multiplier architecture. The coding of multiplier is done on VHDL, synthesis using Xilinx ISE series and implementing using FPGA (SPARTAN-3 FPGA).

REFERENCES

[1] Poornima M, Shivaraj K, Shridhar KP and Sanjay H (2013) 'Implementation of multiplier using Vedic algorithm' International Journal of Innovative Technology and Exploring Engineering, vol. 2, pp. 219-223.

[2] S.S. Soakar, R.M. Banakar and S. Siddamal (2012) 'High speed signed multiplier for digital signal processing applications' IEEE Int. Conf. on signal processing, computing and control, pp. 1-6.

[3] A. K. Itawadiya, R. Mahle, V. Patel and D. Kumar (2013,) 'Design a DSP operation using Vedic Mathematics' IEEE Int. Conf. on communication and signal processing, pp. 897-902.

[4] V. Kunchigi, L. Kulkarni and S. Kulkarni (2012) 'High speed and area efficient Vedic multiplier' IEEE Int. Conf. on devices, circuit and system, pp. 360-364.

[5] David Bbez, David Baa-Villegas, R. Alcantara, J.J. Romero and T. Escalante (2001) A Package For Filter Design Based On Matlab" 31st ASEE / IEEE Frontiers in Education Conference.

[6] Jagadguru Swami Sri Bharath and Krishna Tirathji (1965) 'Vedic Mathematics or Sixteen Simple Sutras from the Vedas' Motilal Banarsidas, Varanasi (India).